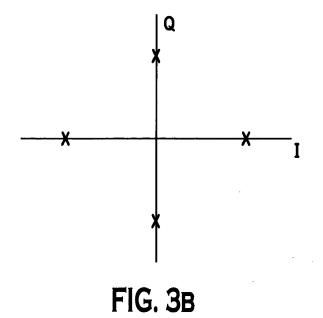


FIG. 3A





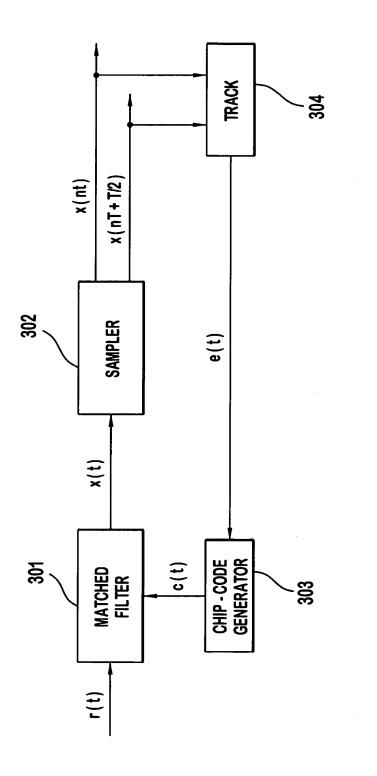


FIG. 30

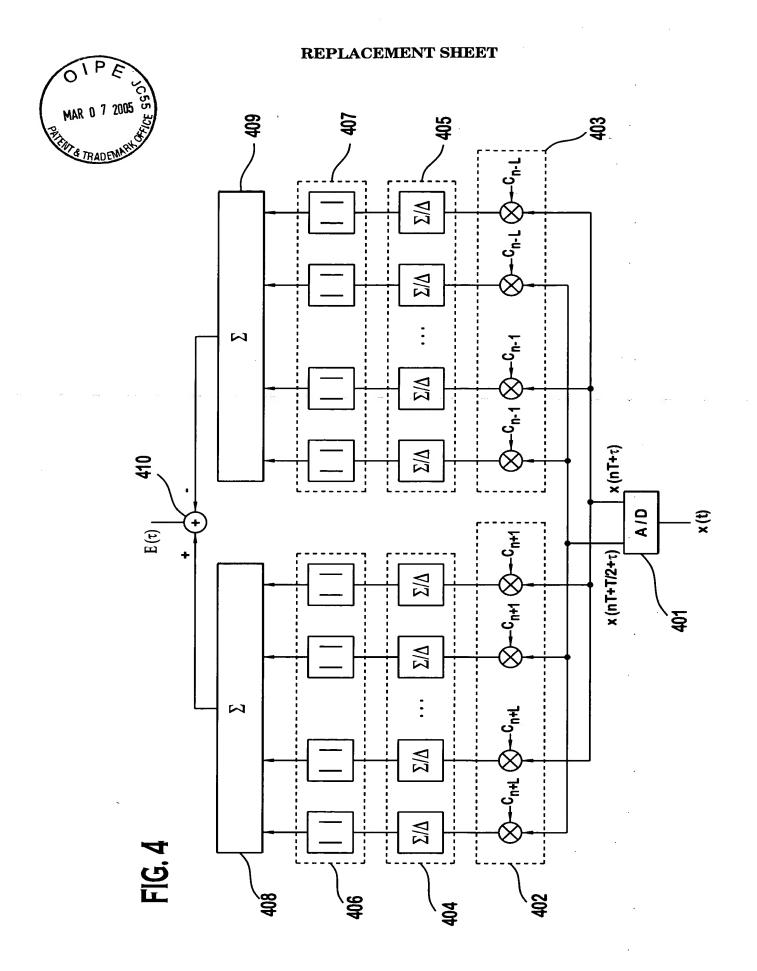
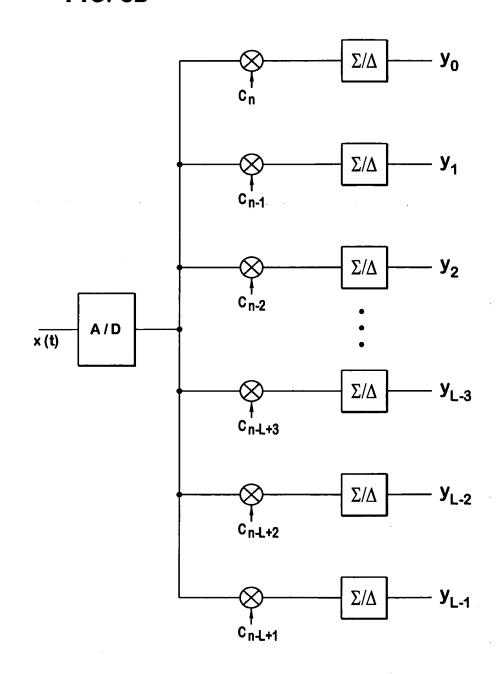




FIG. 5B





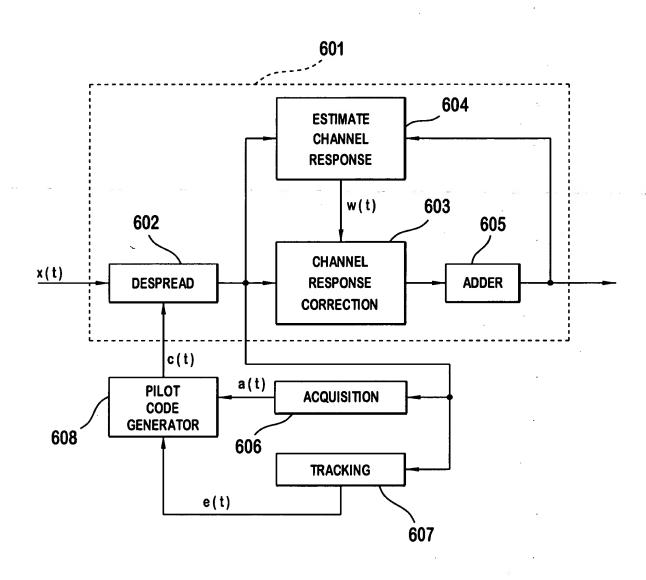
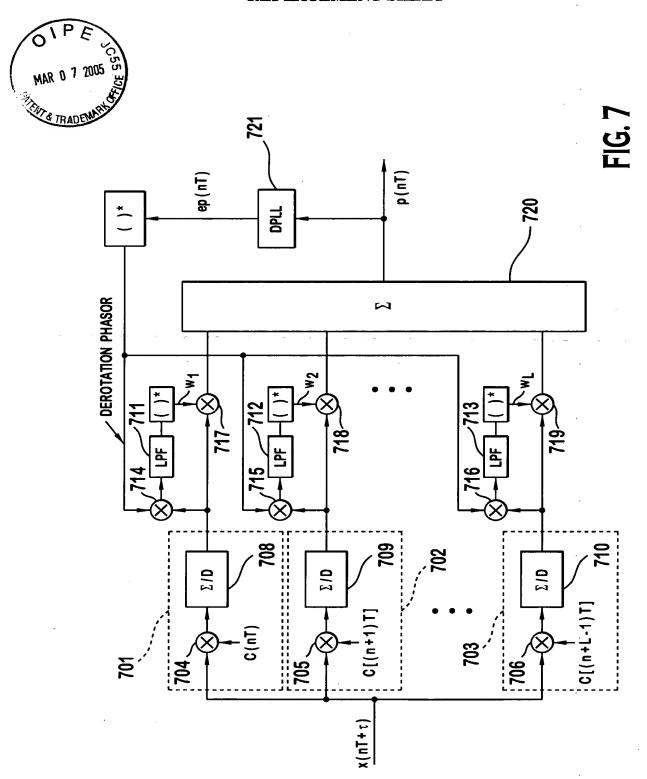


FIG. 6





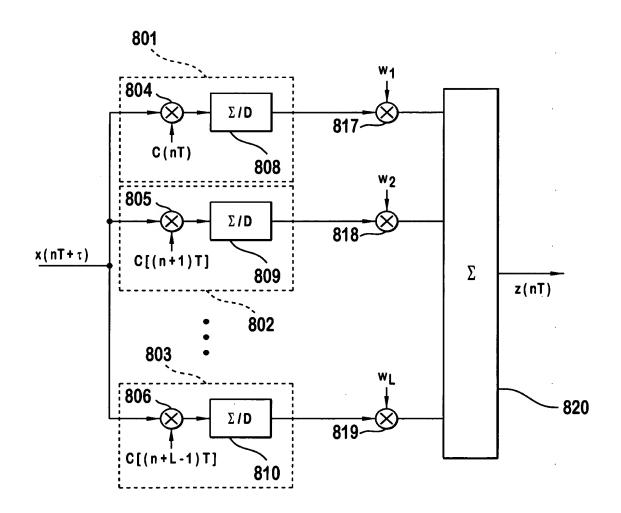


FIG. 8A



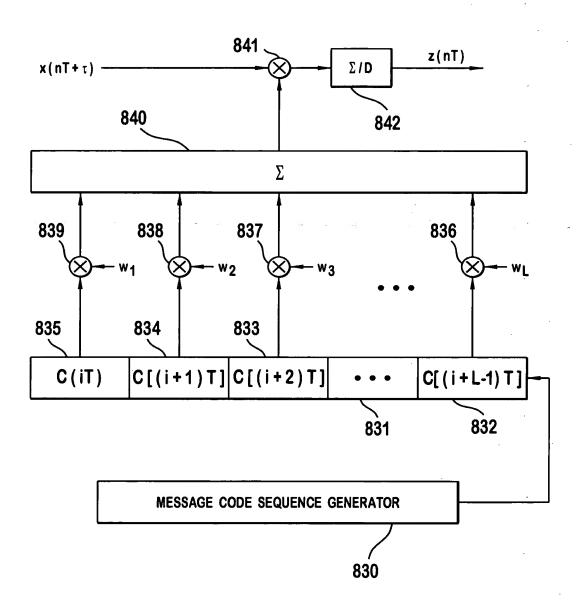


FIG. 8B



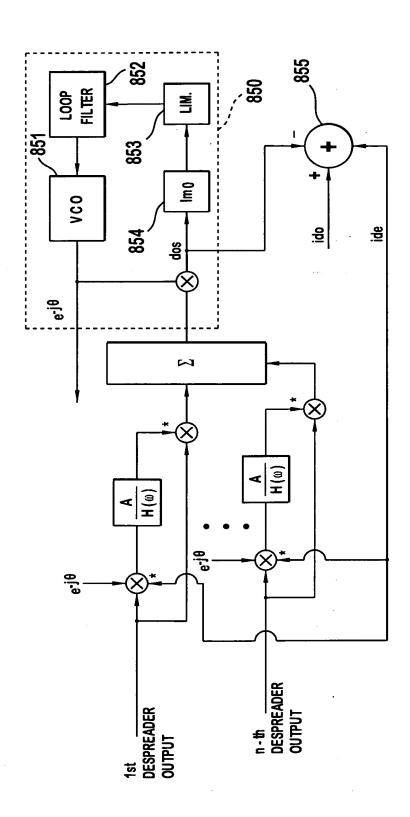
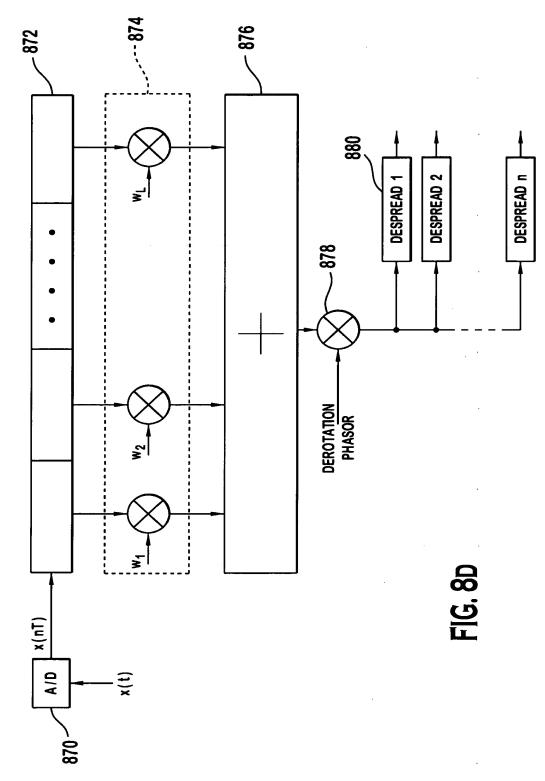
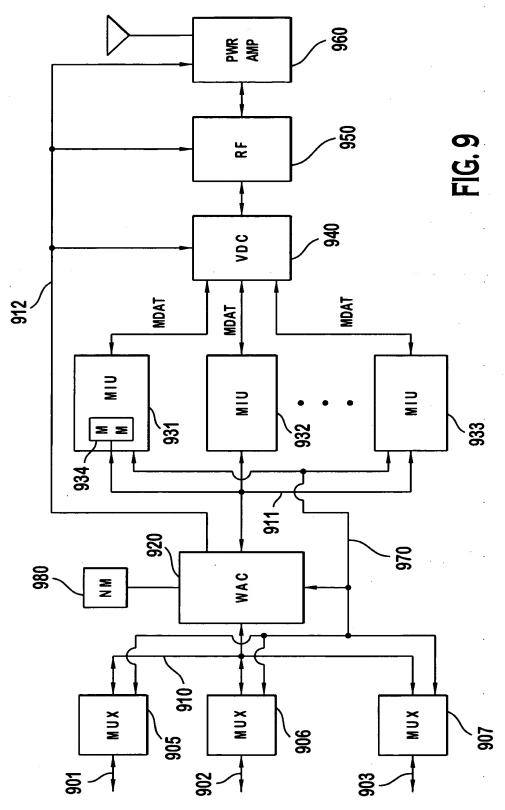


FIG. 80

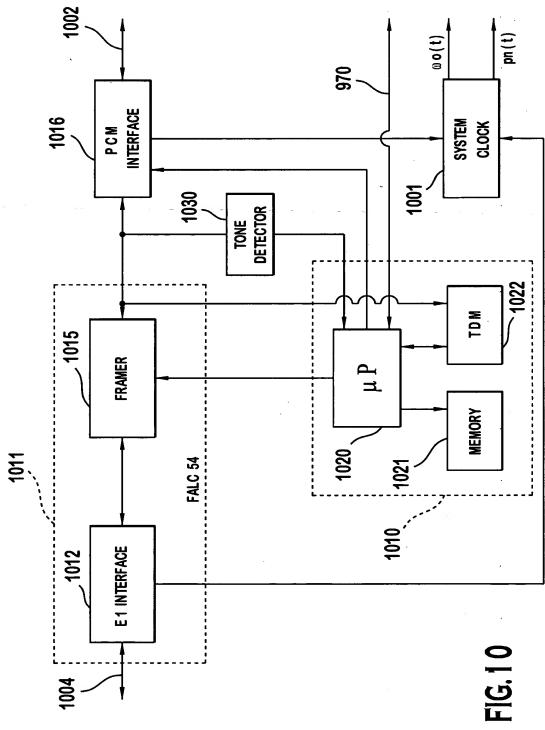




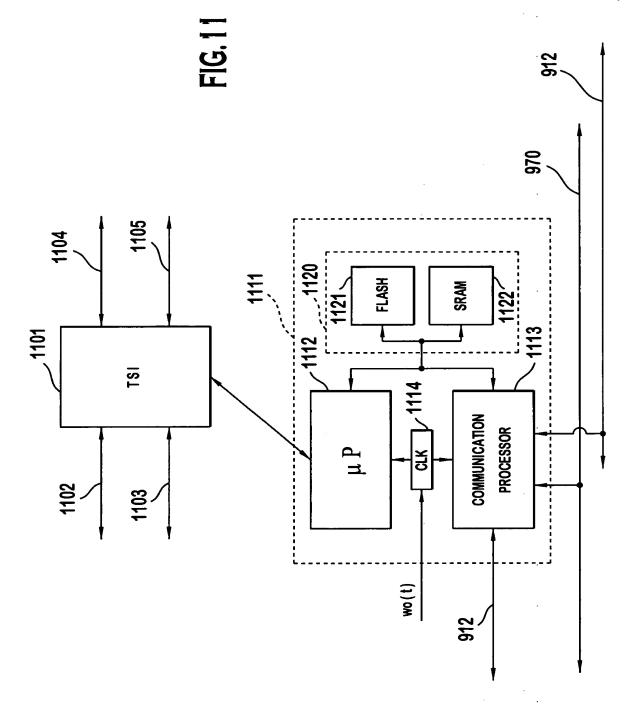




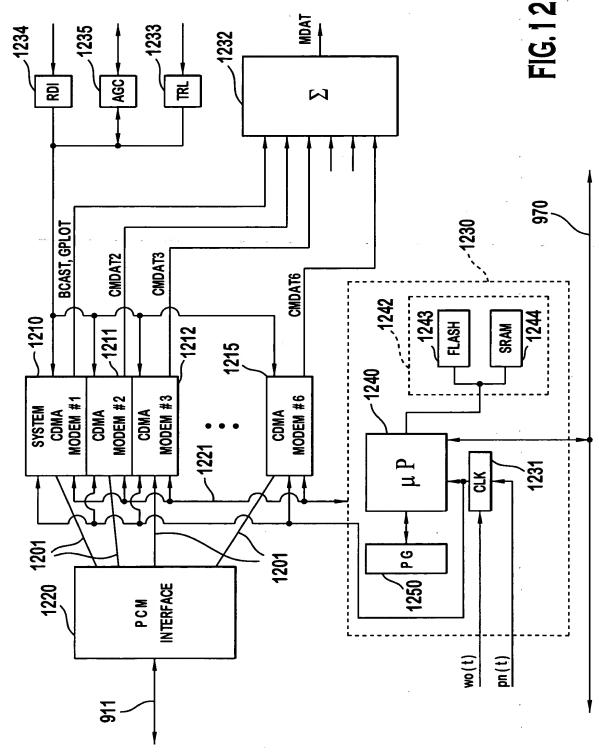














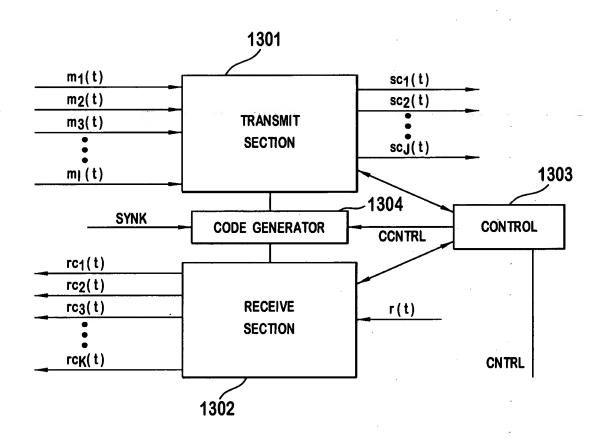
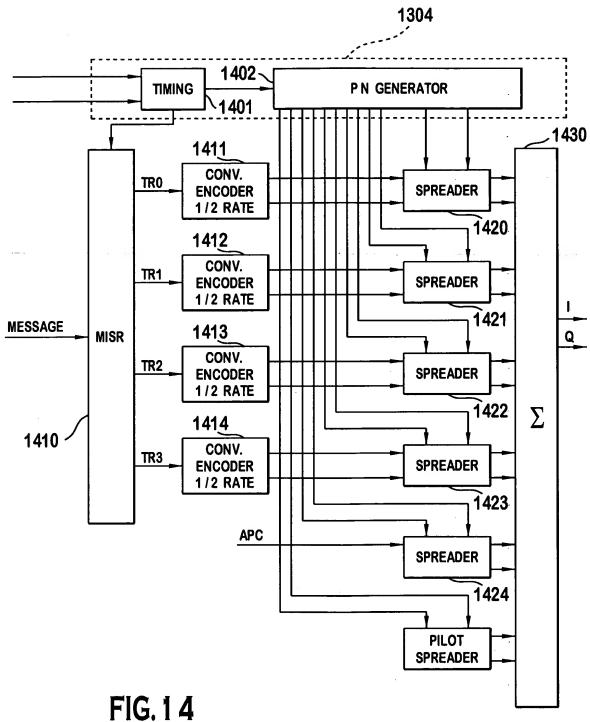
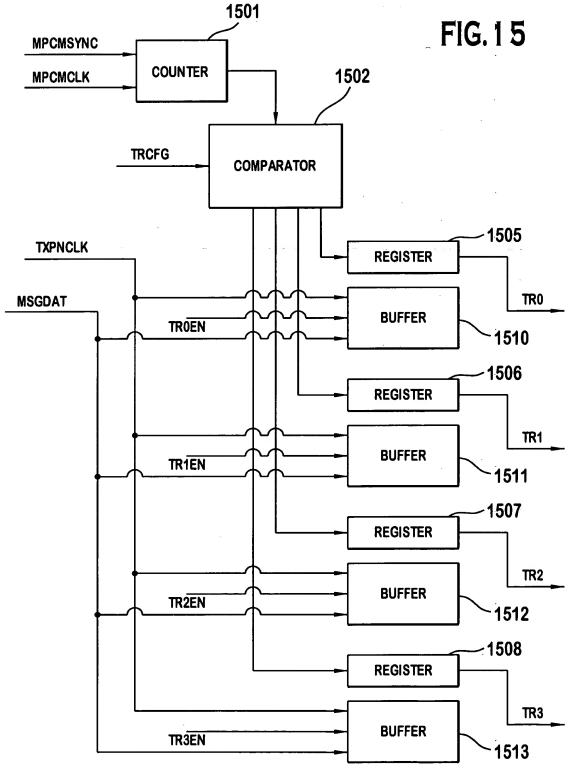


FIG. 13











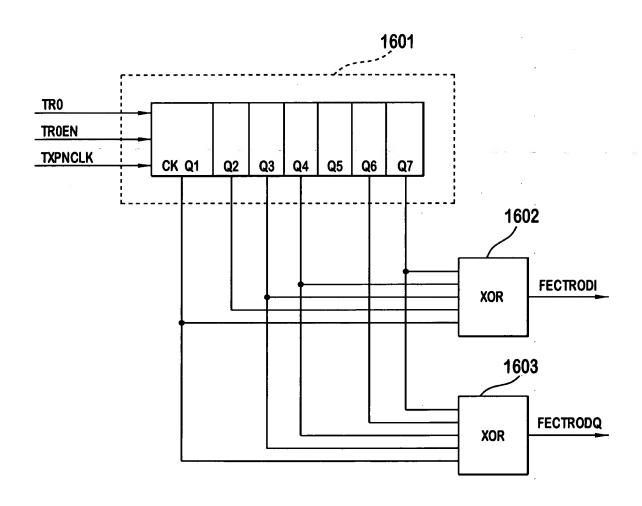


FIG. 16



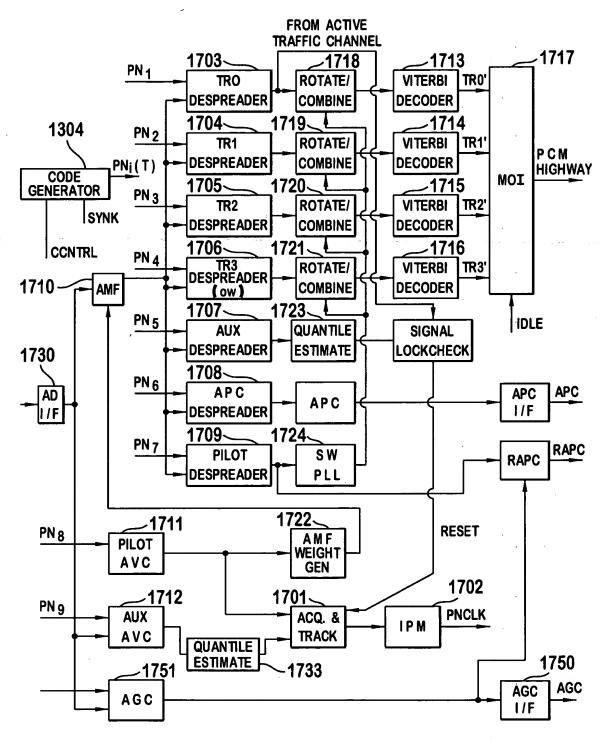


FIG. 17



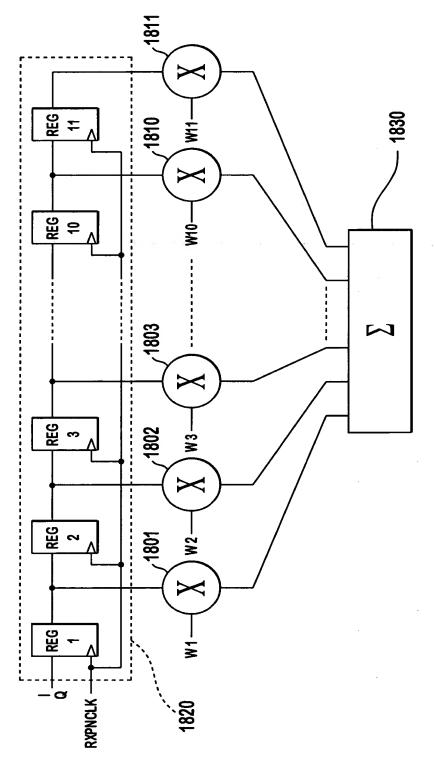


FIG. 18



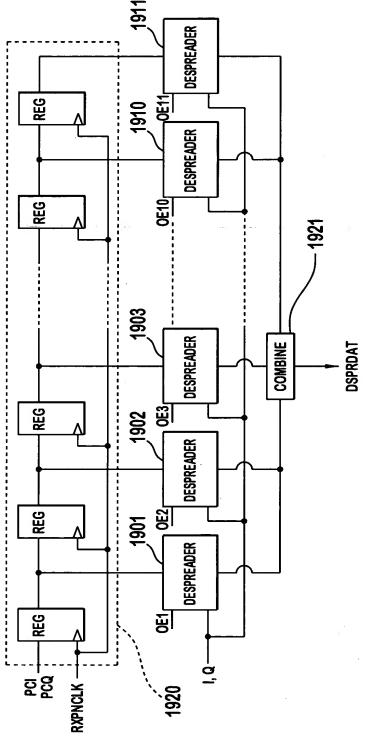


FIG. 19



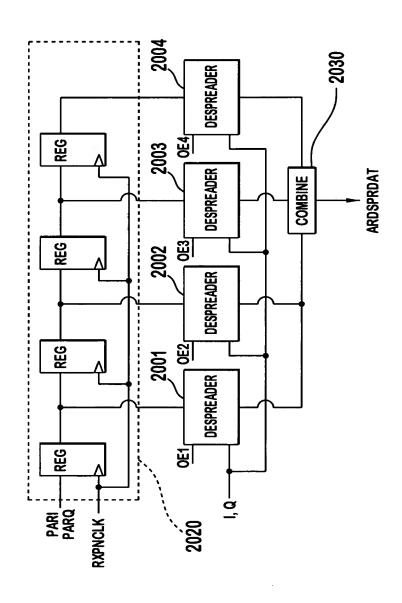
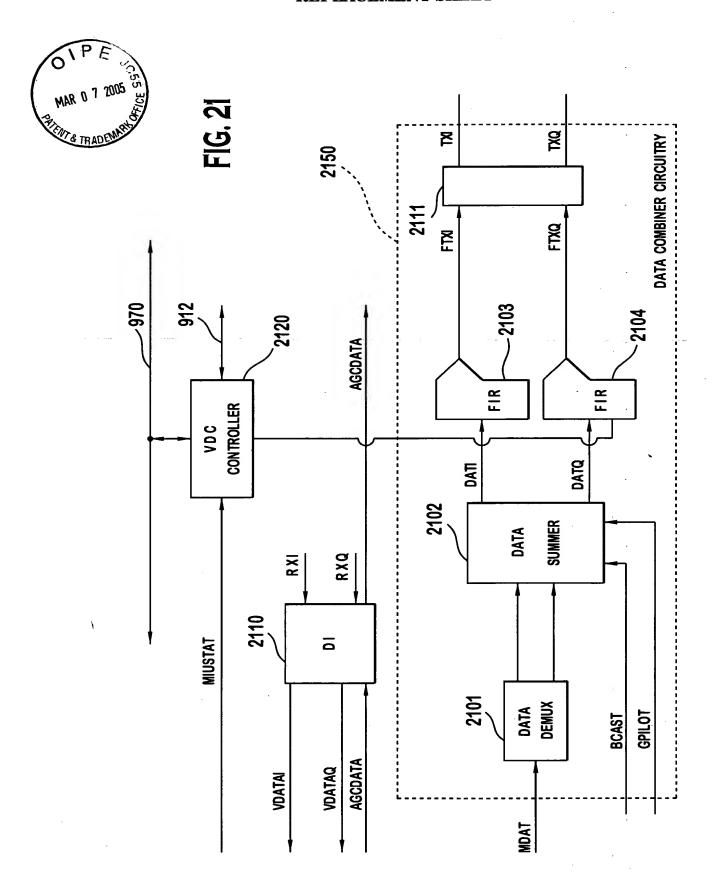


FIG. 20







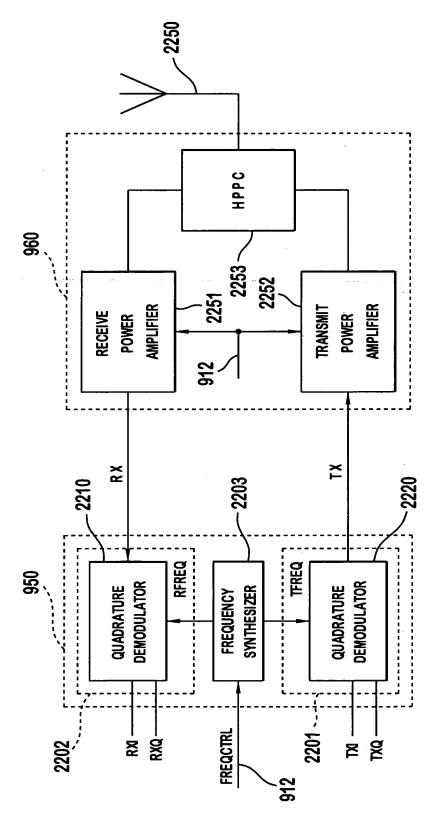
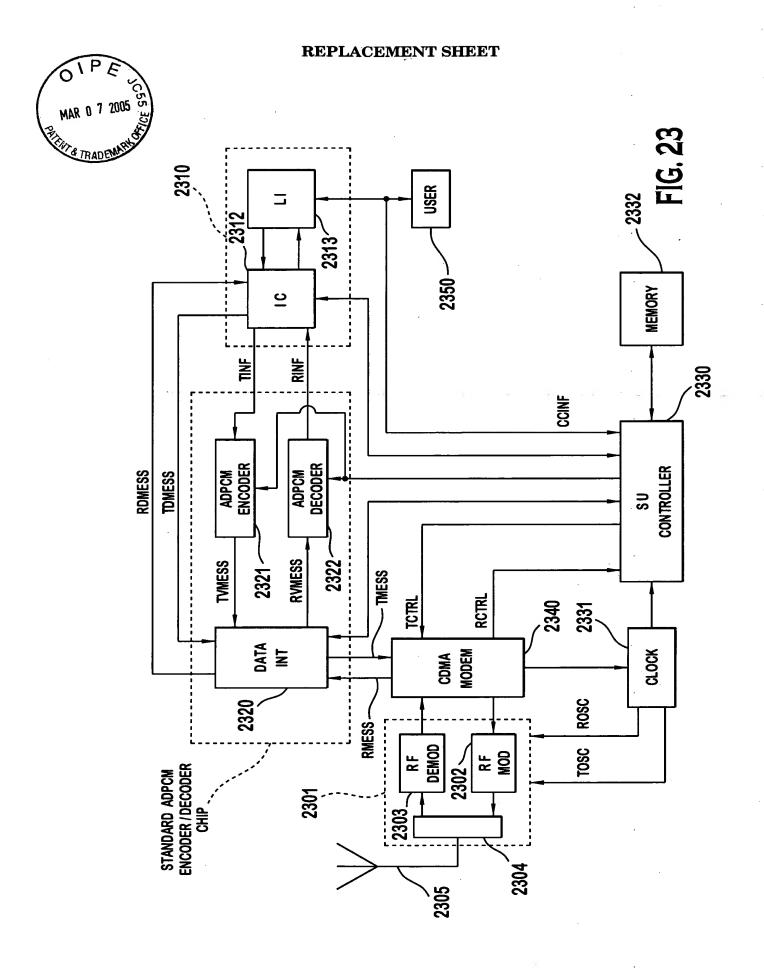
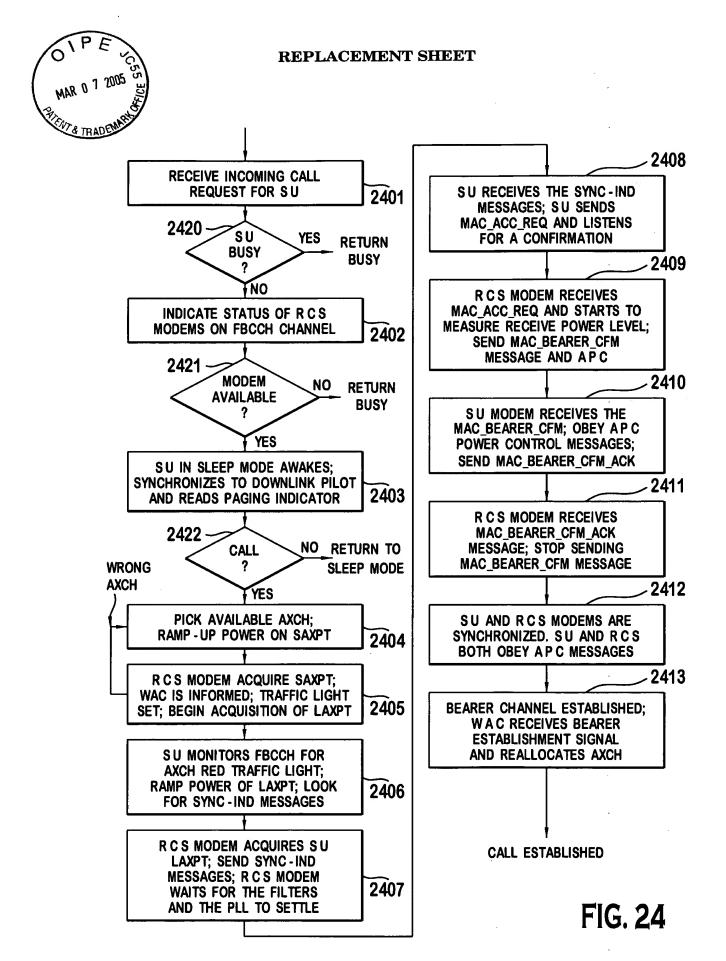
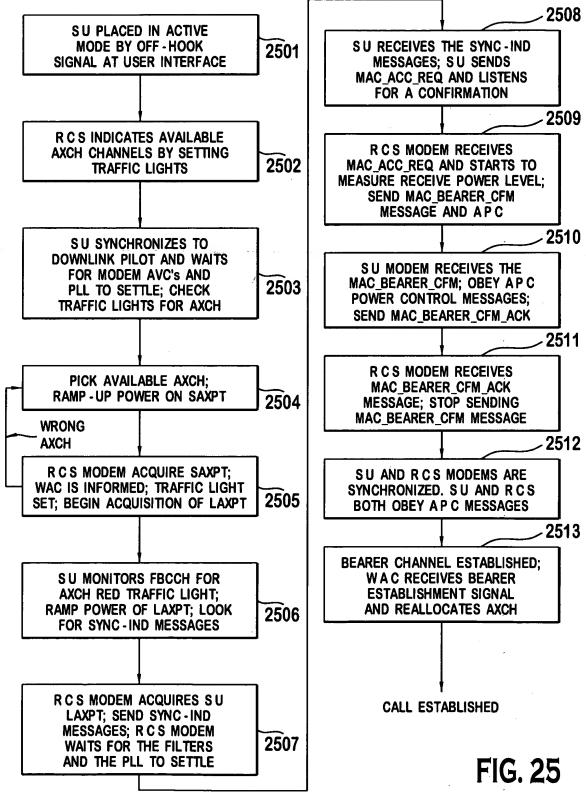


FIG. 22











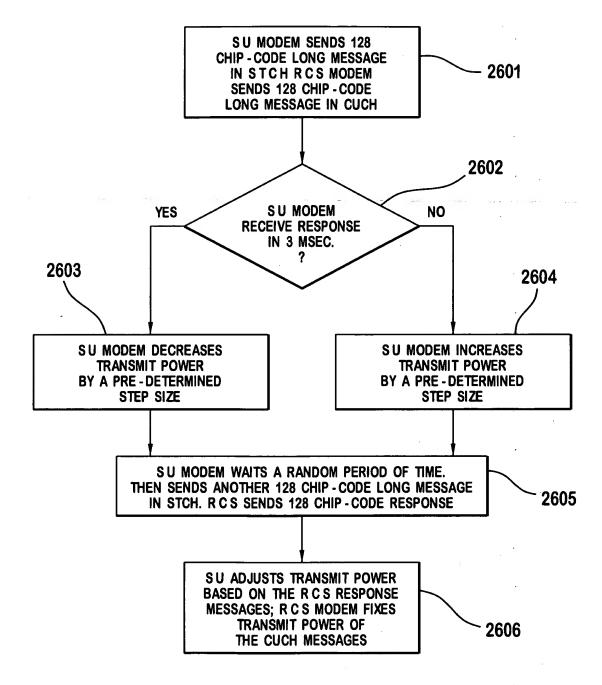


FIG. 26



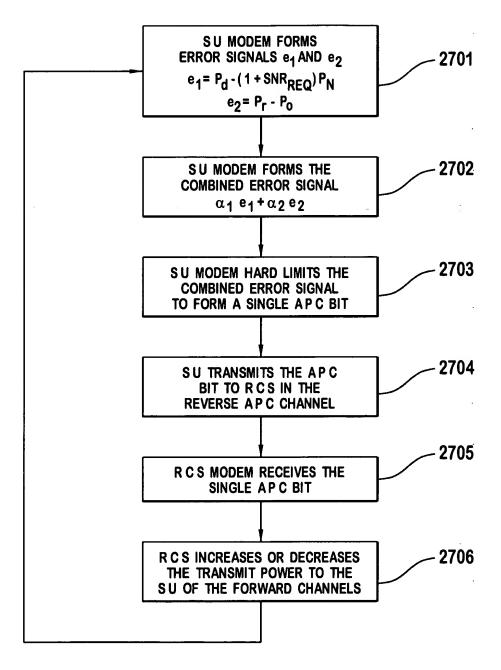


FIG. 27



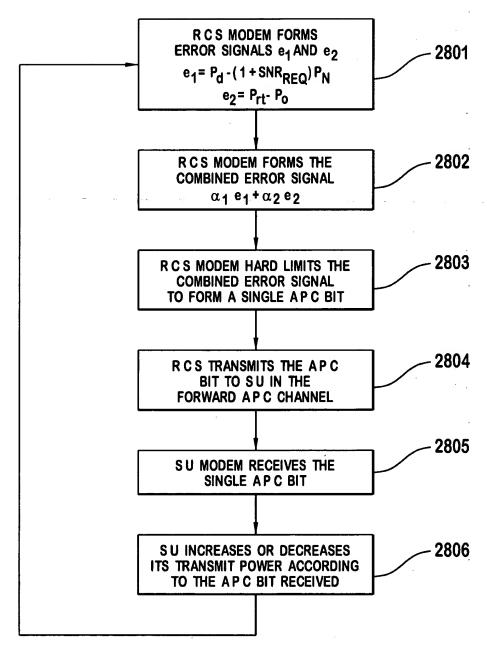
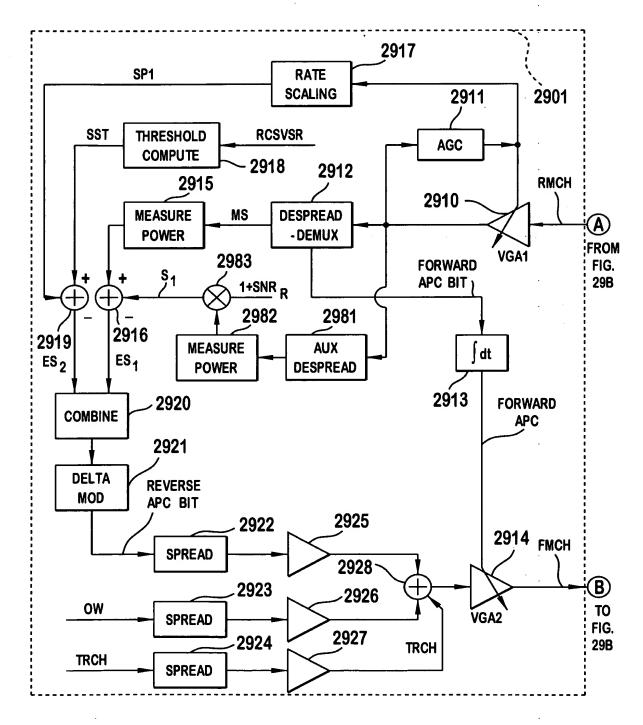


FIG. 28



FIG. 29A





# FIG. 29B

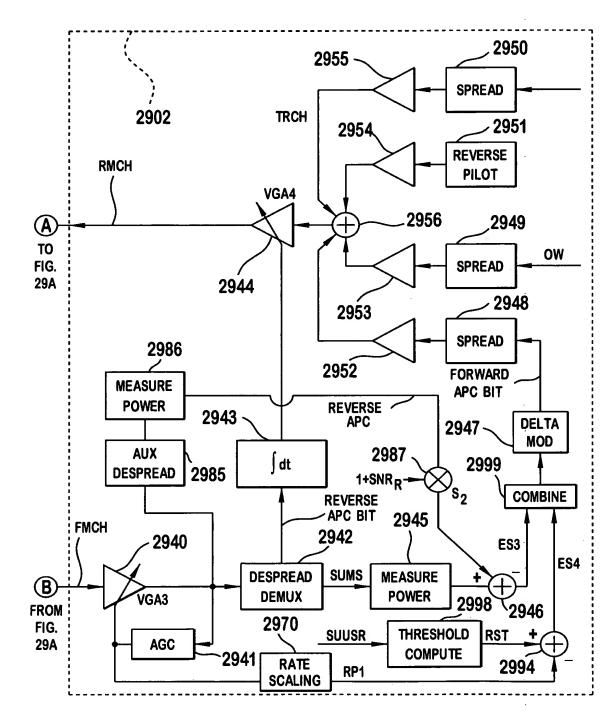
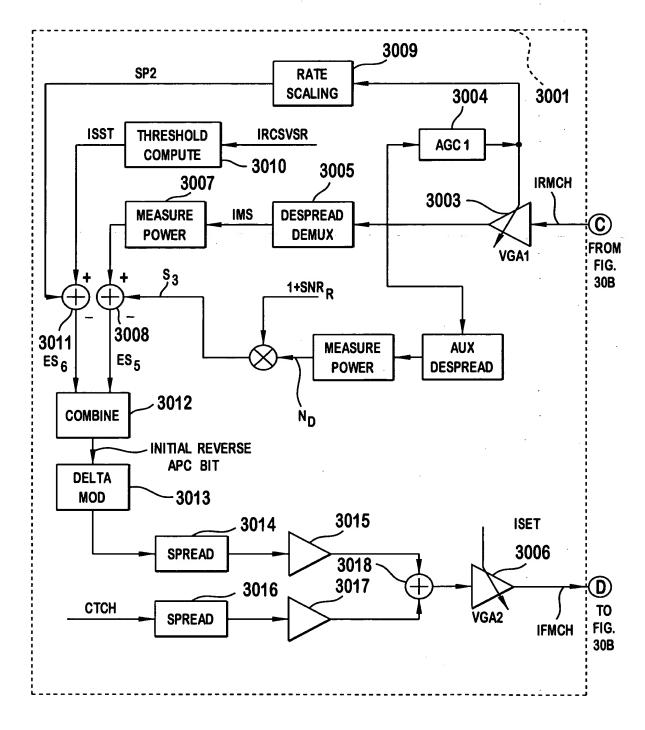




FIG. 30A





# FIG. 30B

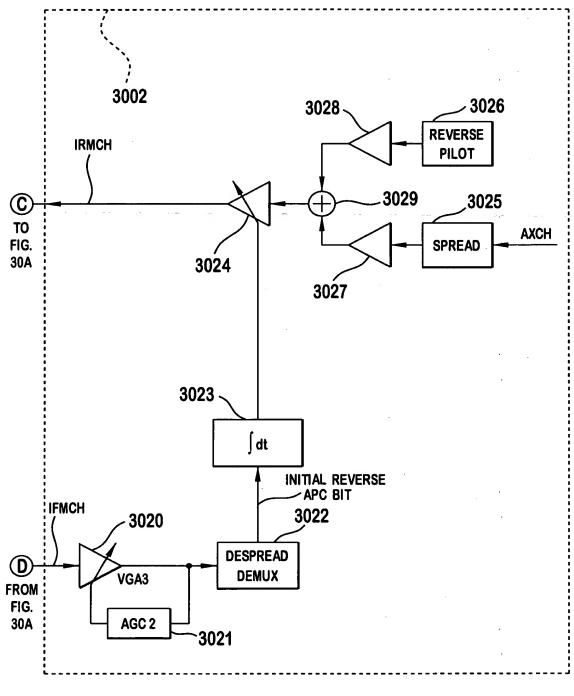




FIG. 31

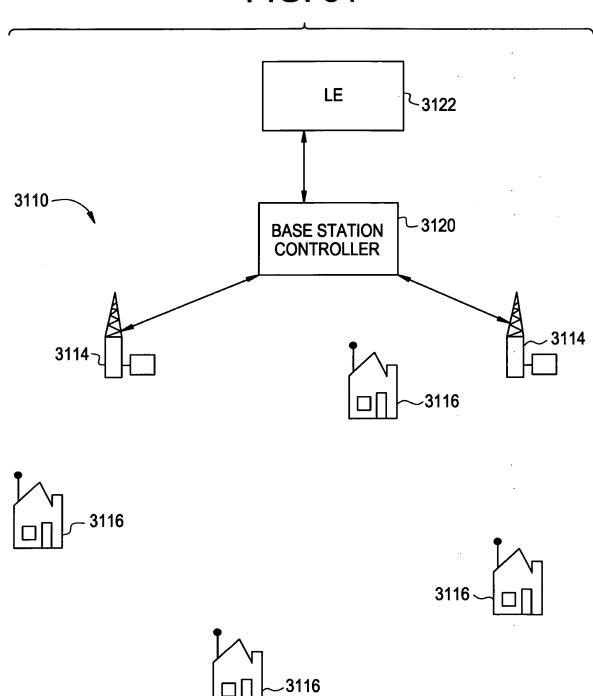
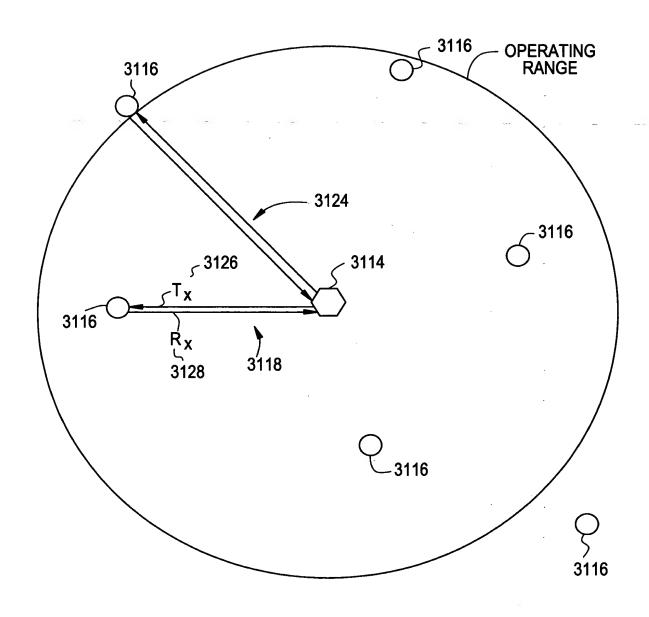




FIG. 32





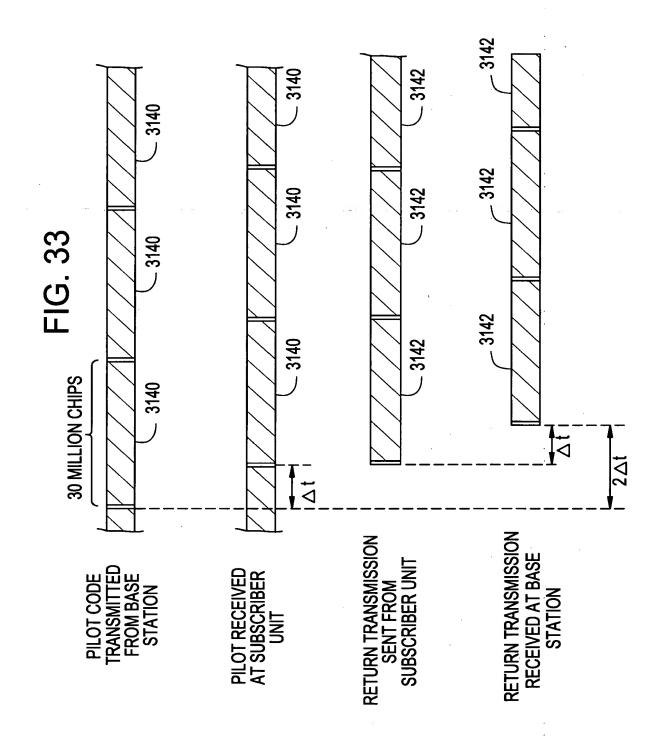
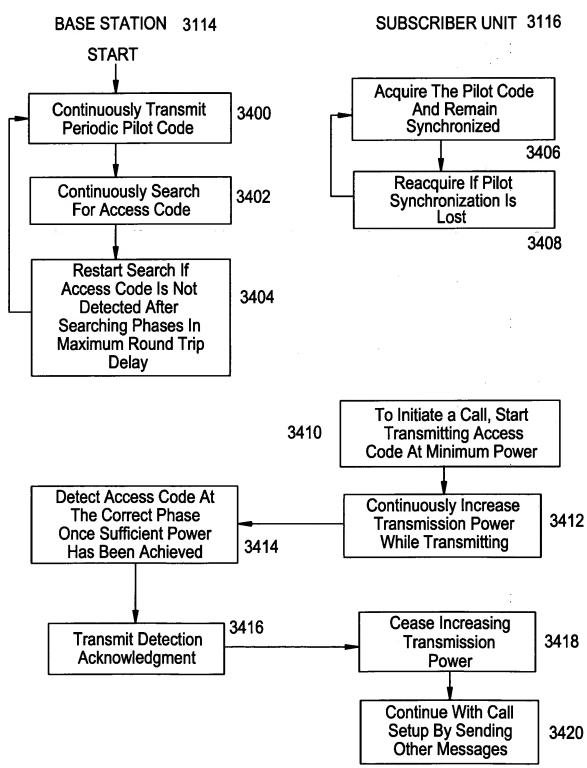




FIG. 34





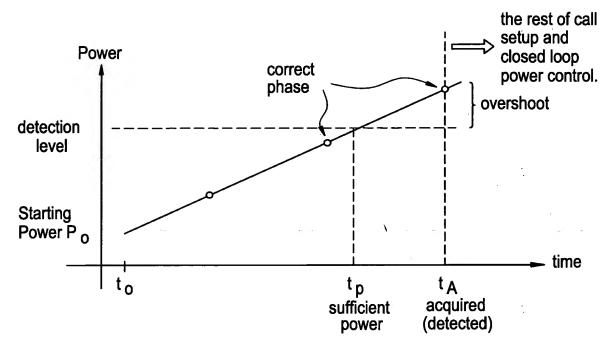
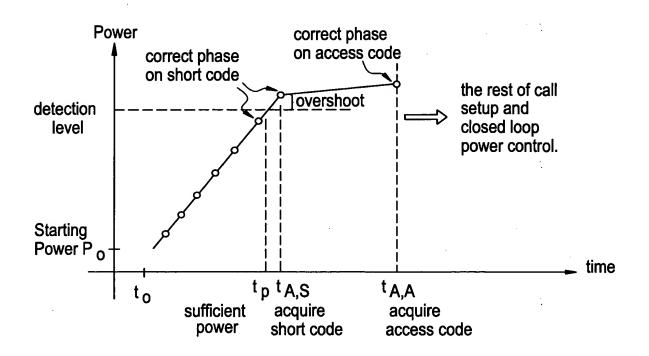
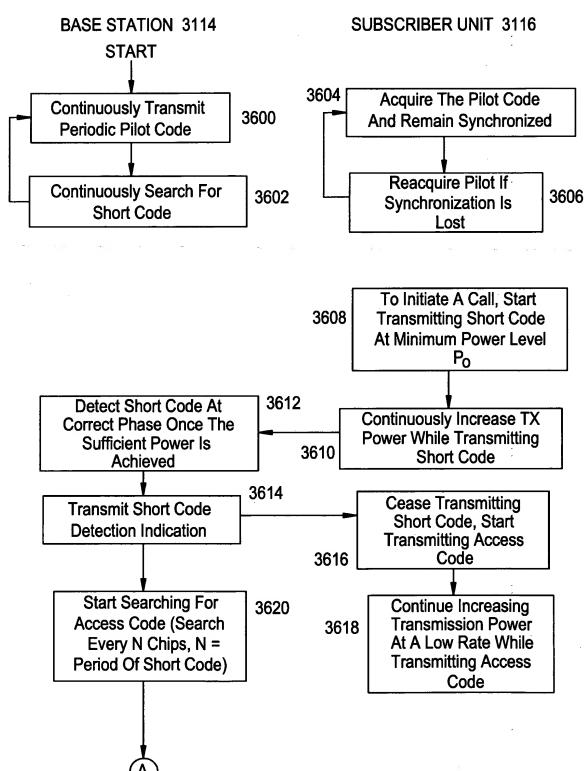


FIG. 37



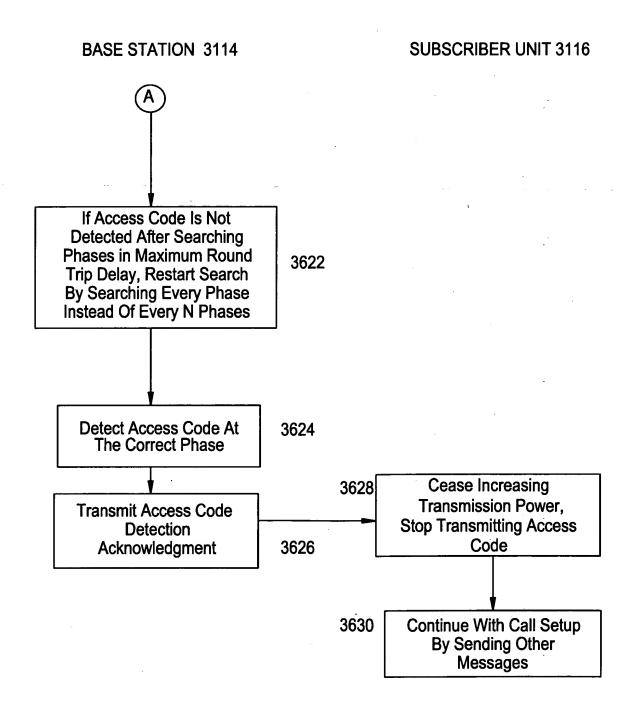


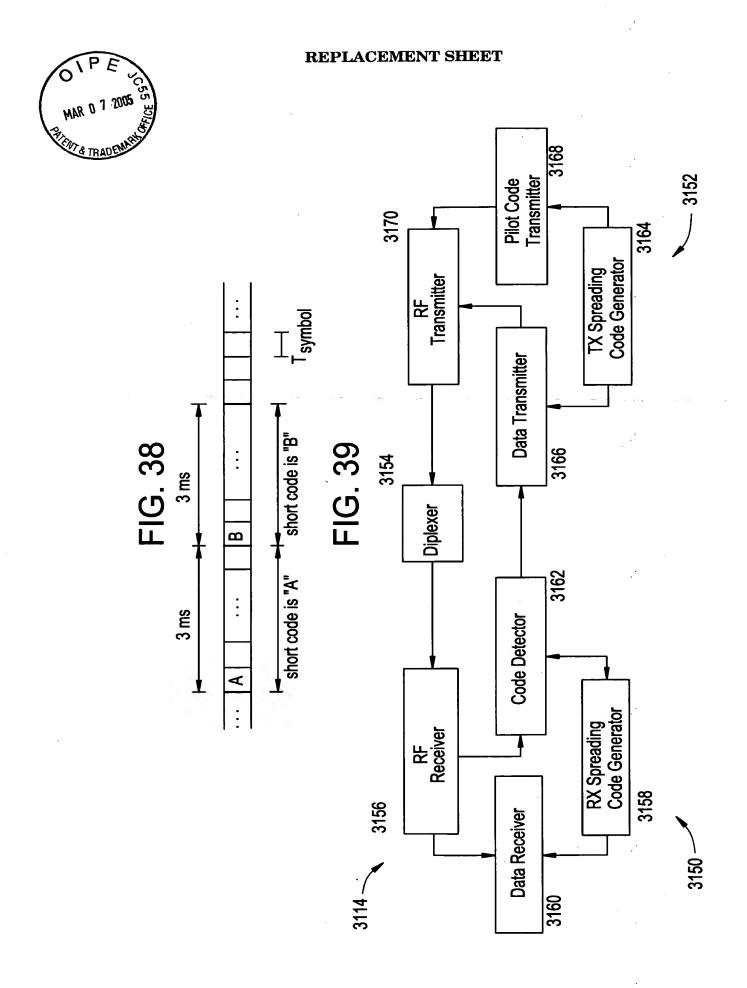
## **FIG. 36A**



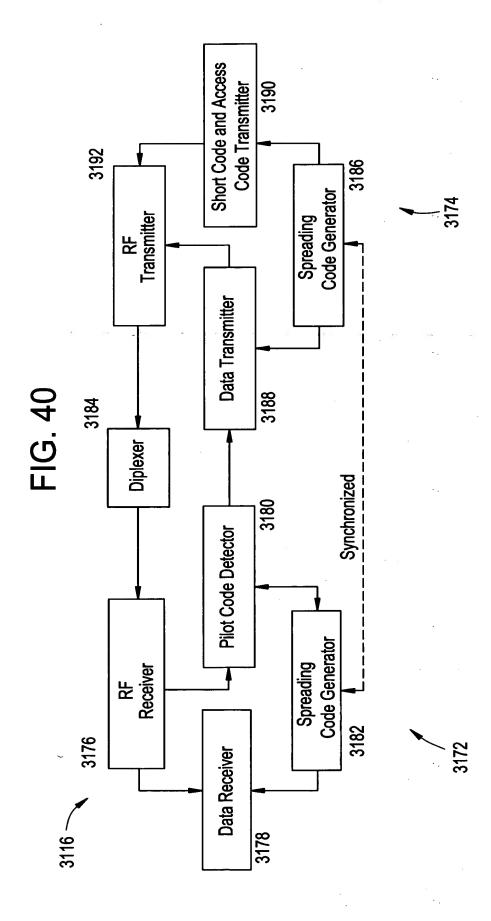


## FIG. 36B



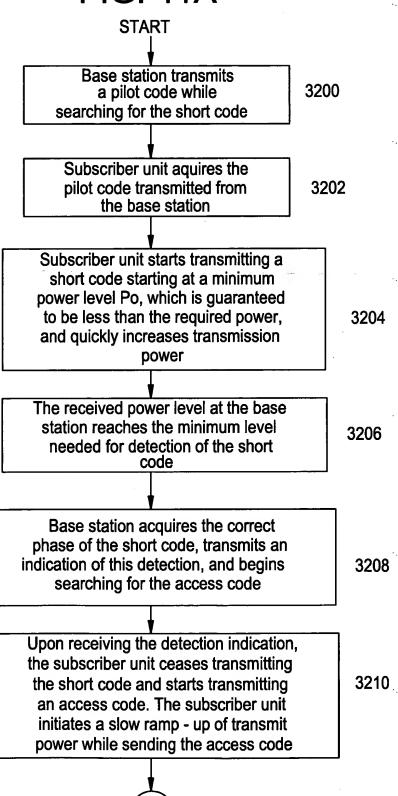








## **FIG. 41A**





## **FIG. 41B**



Base station searches for the correct phase of the acces code by searching only one phase out of each short code length portion of the access code

3212

If the base station searches the phases of the access code up to the maximum round trip delay and has not detected the correct phase, repeat search by searching every phase

3214

Upon detection of the correct phase of the access code by the base station, the base station sends an acknowledgement to the subscriber unit

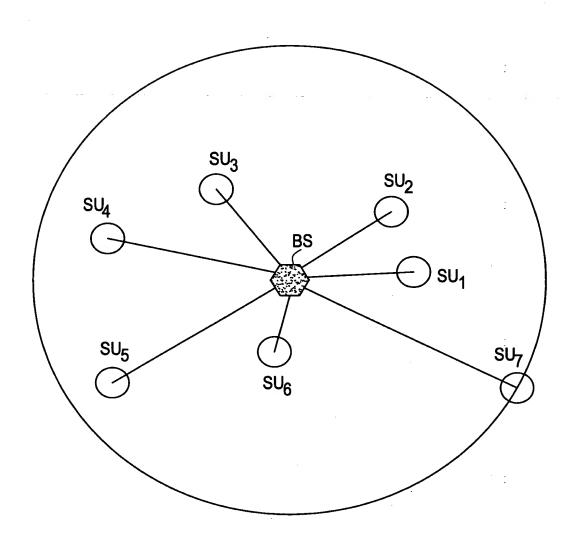
3216

Reception of the acknowledgment by the subscriber unit concludes the ramp - up process. A closed loop power control is established, and the subscriber unit continues the call setup process by sending related call setup messages

3218



FIG. 42 PRIOR ART





## FIG. 43 PRIOR ART

Mean Cell Sweep Time, FSU @ 20 KM

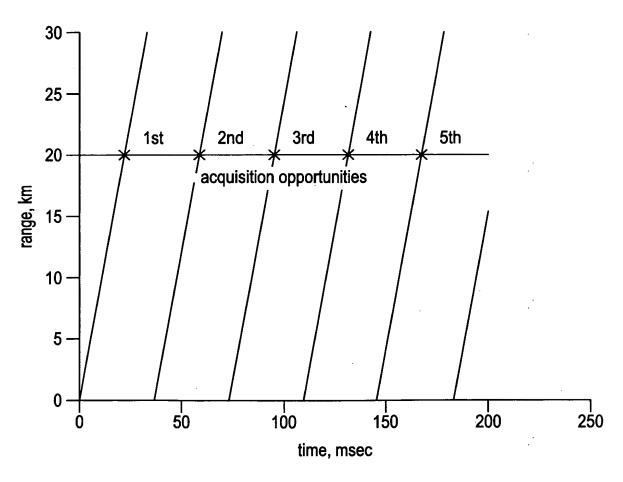




FIG. 44

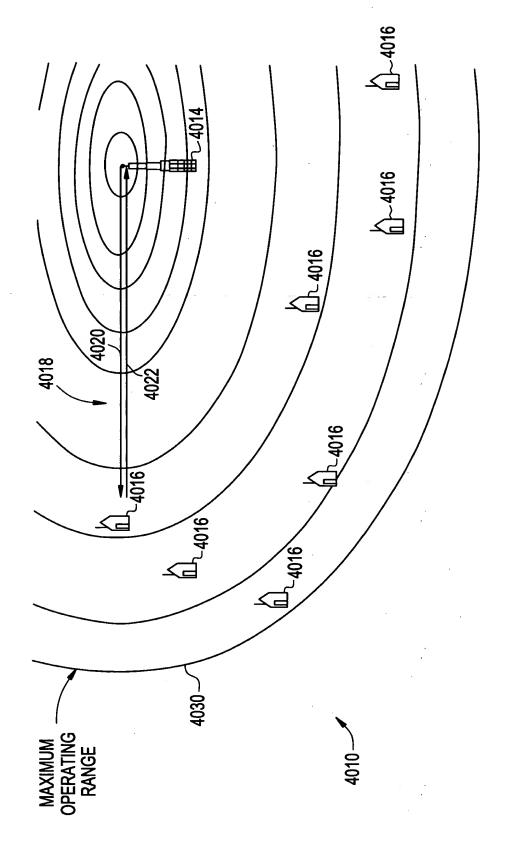




FIG. 45

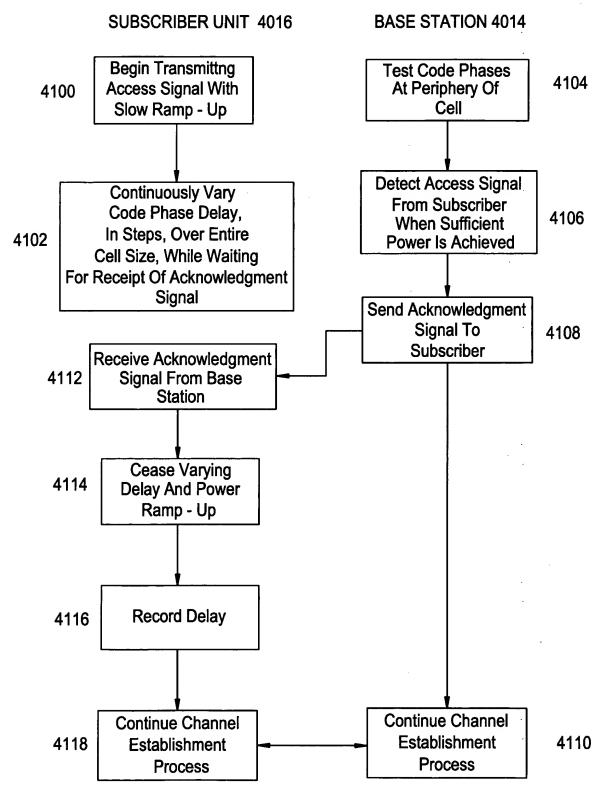
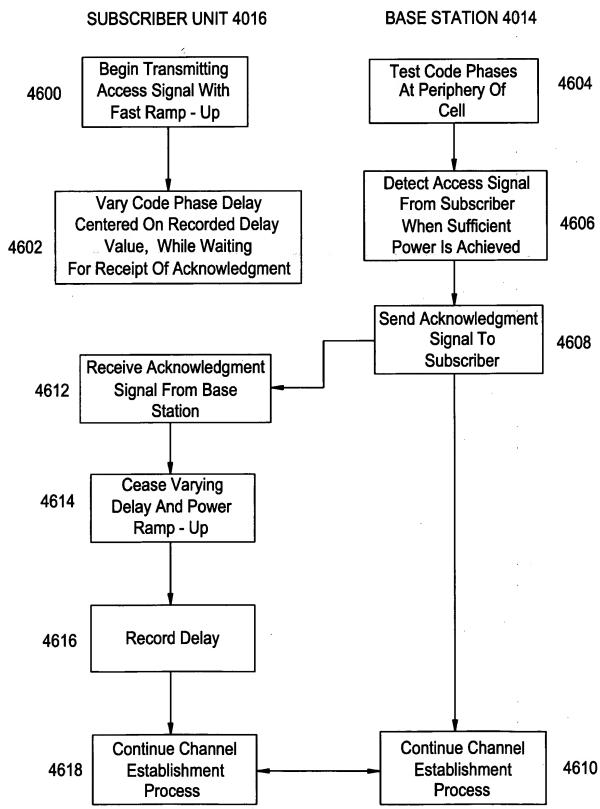
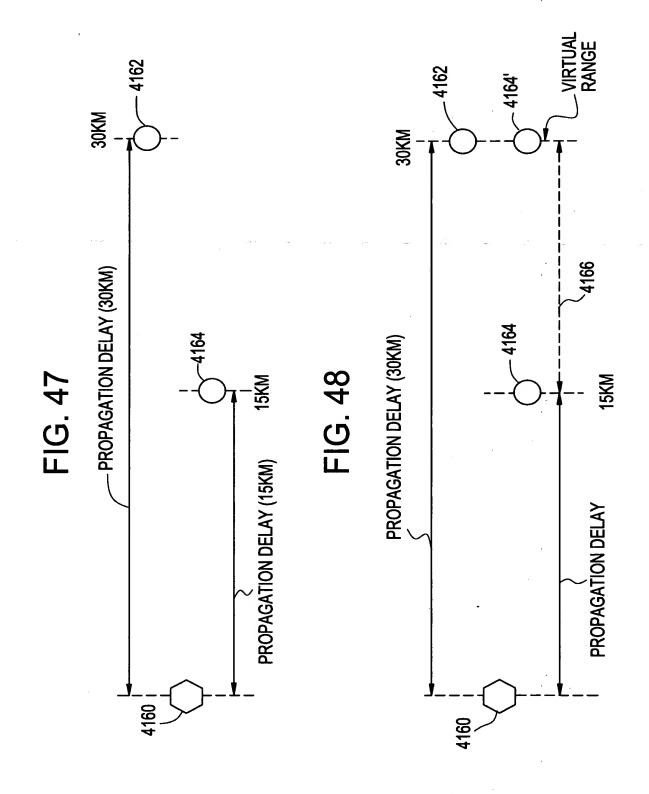




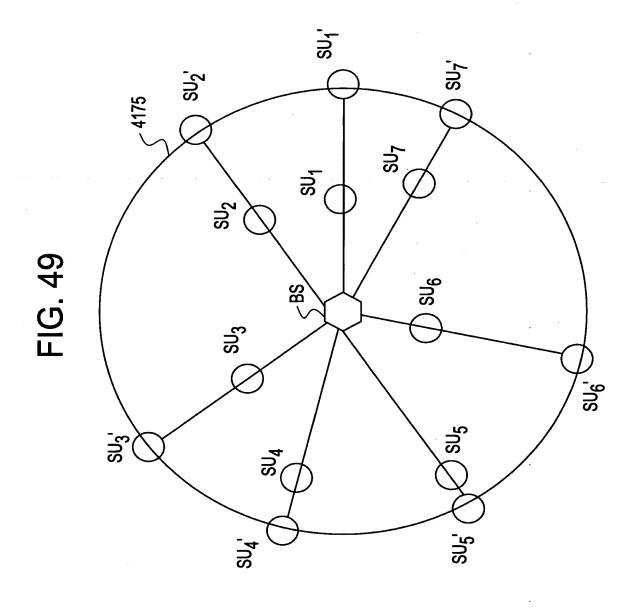
FIG. 46



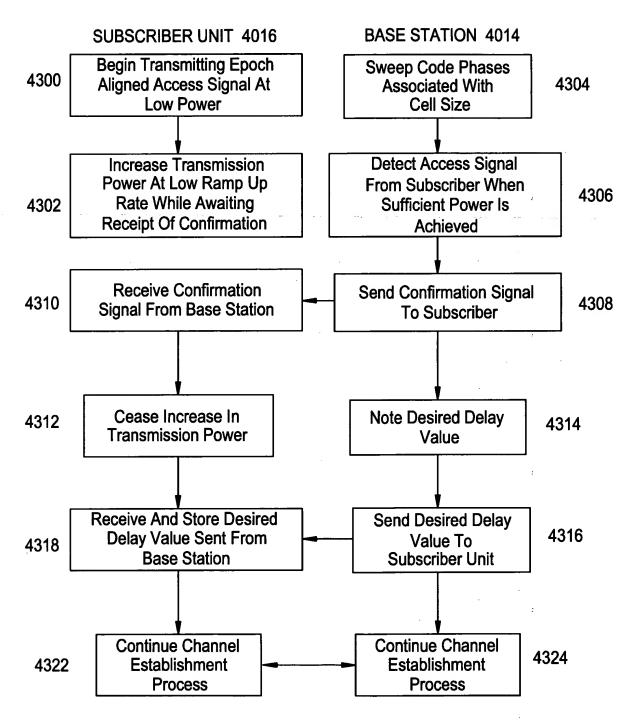




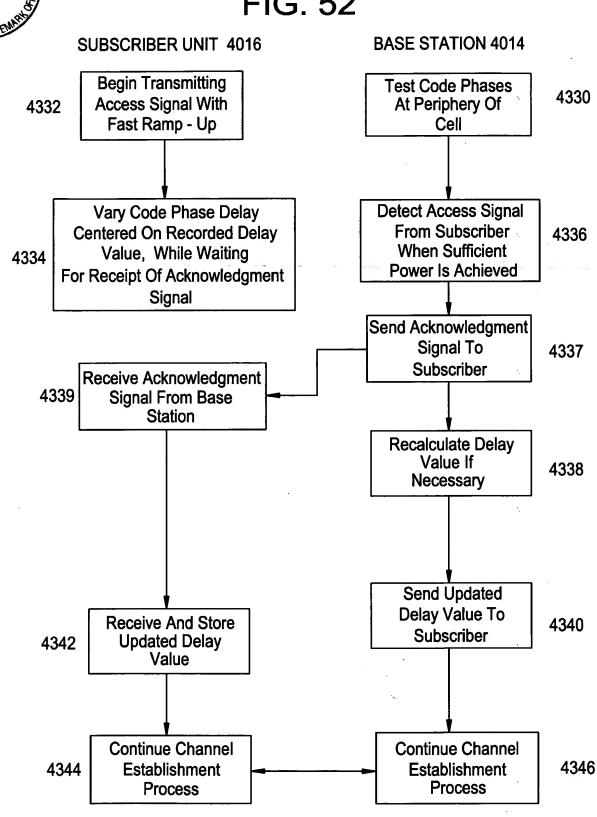




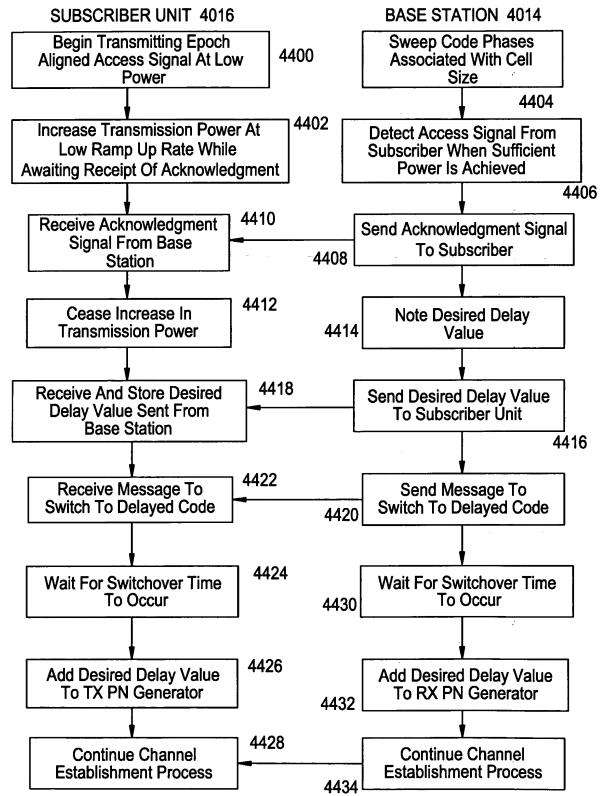






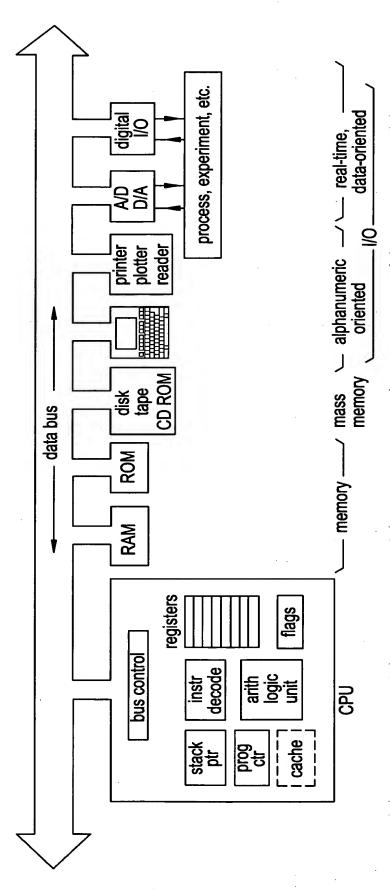












#### REPLACEMENT SHEET



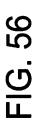
FIG. 55 PRIOR ART

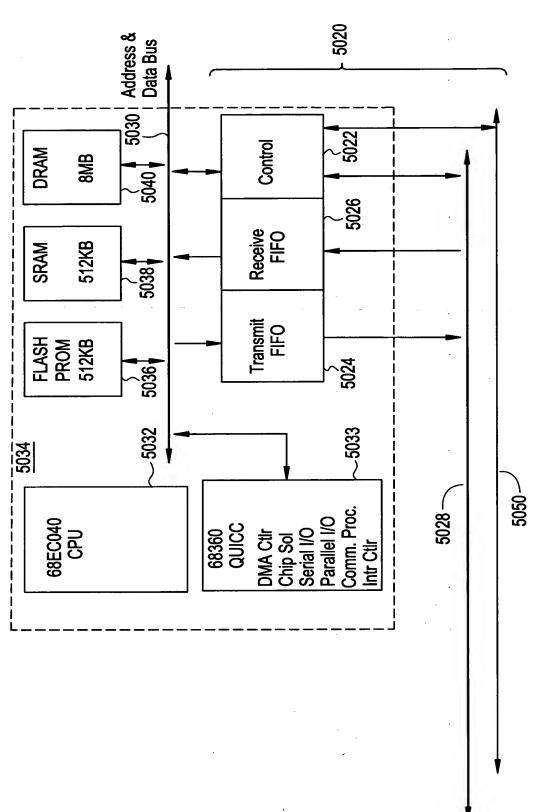
Comments	controller-type applications	original IBM PC & compatibles	accepts PC/XT cards	enhanced PC/AT; auto-configure	IBM PS/2; auto-configure	LSI-11, LVAX-I, II; daisy-chained IACK	Intel; SUN-I and others	data acqusition & control bus	VAX 780, 8600 series; parity	parity; 40MB/s for blk xfer, 20M otherwise	Macintosh II adds 1 dedicated INT per slot: "	daisy-chained IACK; SUN-3		communication across many crates
Connector b	_	띵		띵	띵									I
Drivers	H	E	Ħ	É	Ę	<b>©</b>	Ę		E	E	Ę	E	<del>©</del>	EC.
IRQ Lines a	_	25	16	<del>1</del>	<del>-</del>	4	∞	_	4	Σ	Σ	_	ı	Σ
Sync/Async	တ	ഗ	ഗ	ഗ	4	⋖	⋖	ഗ	ഗ	ഗ	ഗ	4	⋖	⋖
Multimaster?	1	1	<u>ပ</u>	•	•	•	•	I	•	•	•	•	•	•
MUXed data/adr?	1	1	1	1	I	•	I	I	•	•	•	I		•
Block xfer?	ı	I	I	•	•	•	I	•	•	•	•	•		•
Address width	16	20	20,24	20,24,32	24,(32)	22	20,24	တ	32	16,32	35	16,24,32		32
Data width	8	œ	8,16	8,16,32	8,16,(32)	16	8,16	<b>5</b> 4	8,16,24,32	8,16,24,32	35	8,16,32		32
RAW bandwidth (Mbyte/s)									•			육		
BUS	STD bus	PC/XT	PC/AT	EISA	MicroChanne	Q-bus	Multibus I	CAMAC	VAX BI	Multibus II	NuBus	VME.	Futurebus -	Fastbus

(a) E-edge-sensitive;L-LAM ("look at me");M-"int" via bus mastership; P-programmable edge-or level-sensitive interrupts.

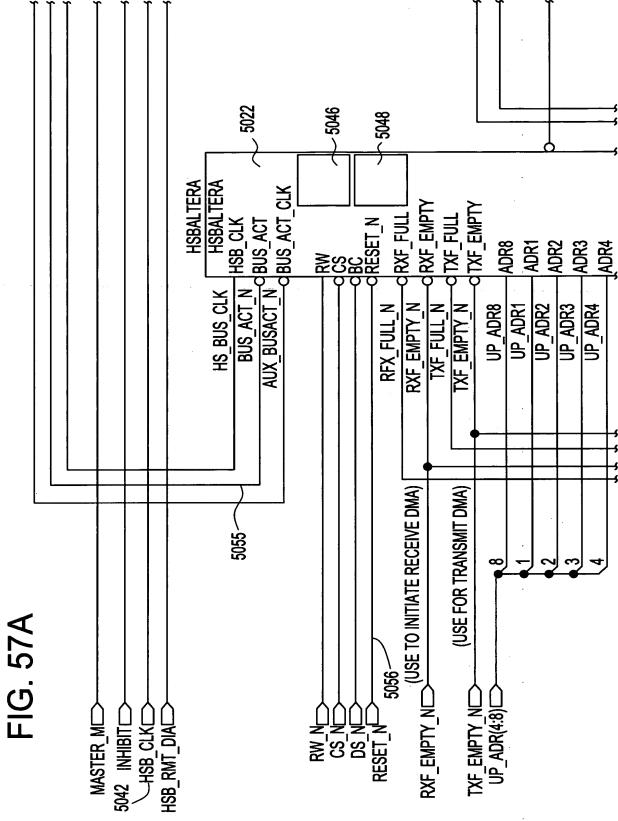
 (b) CE-card-edge; DIN-2-part "Eurocard" 96-pin connector; H-high density 2-part conn. (c) almost. (d) National Semi special

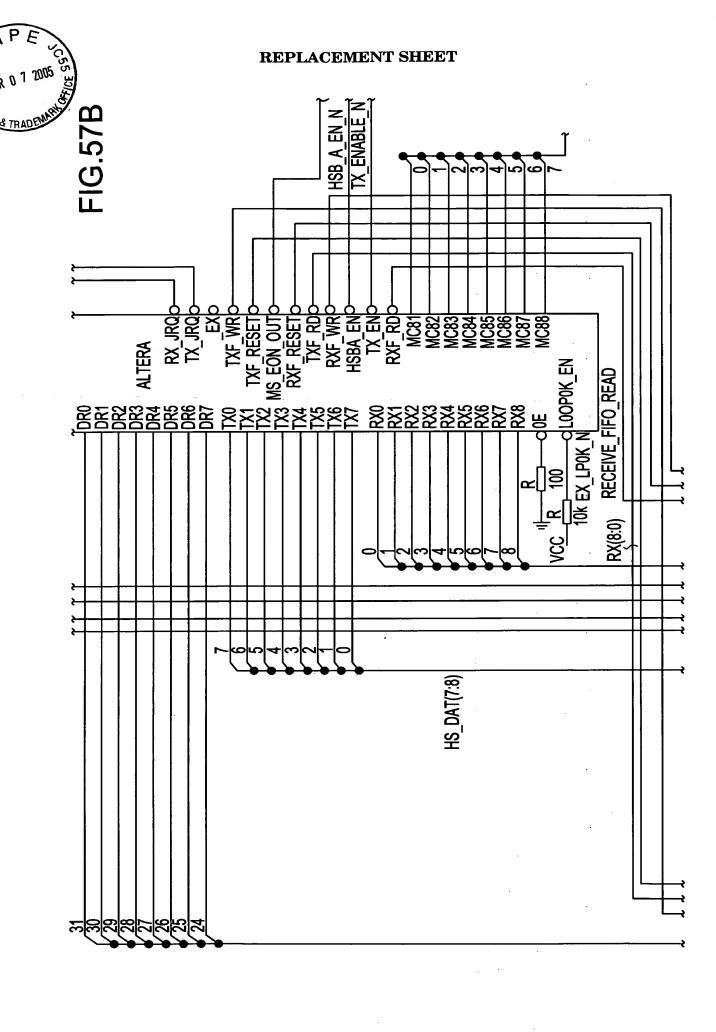














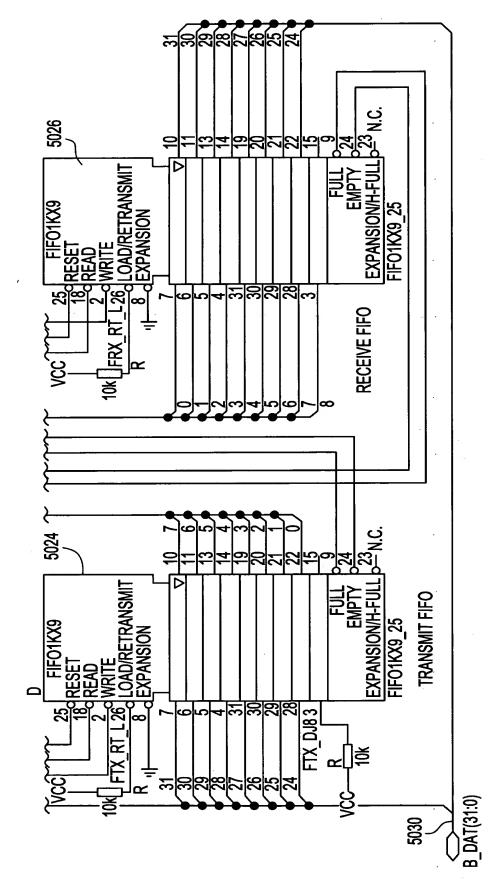
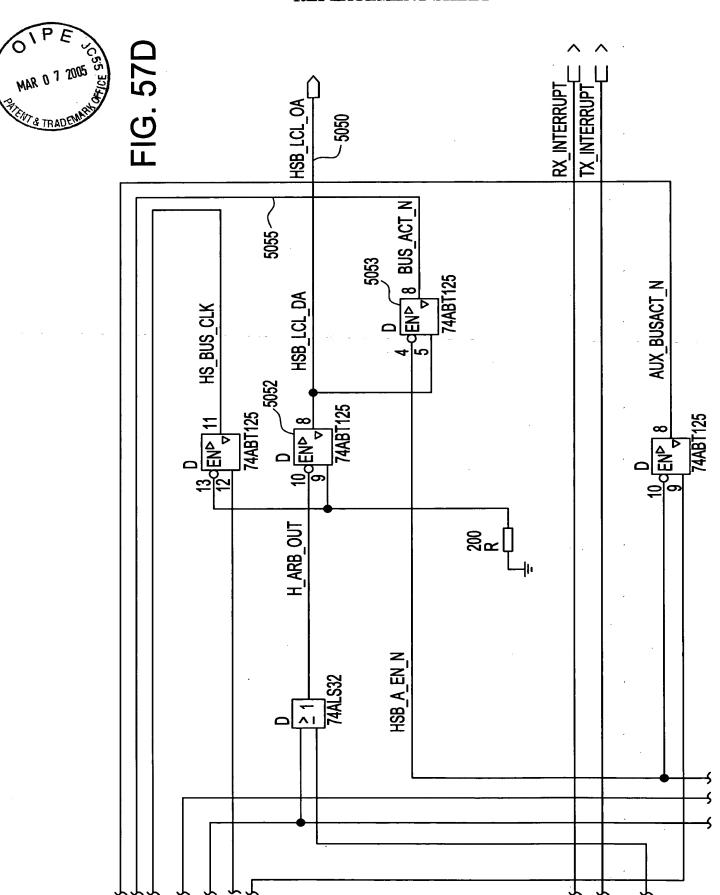
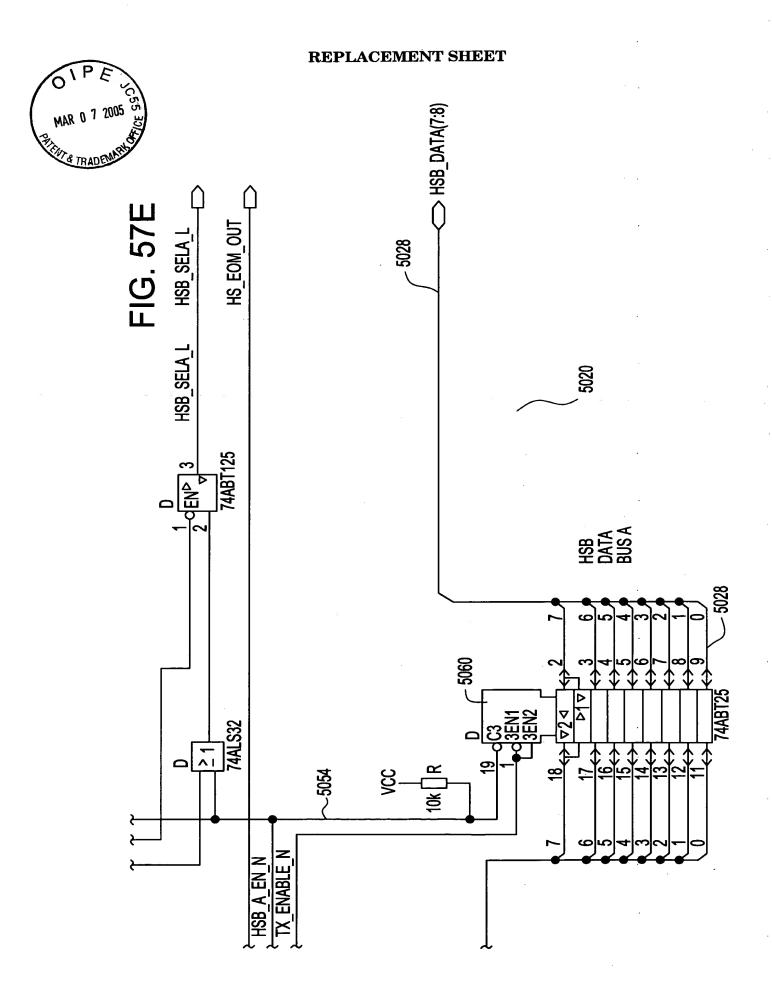
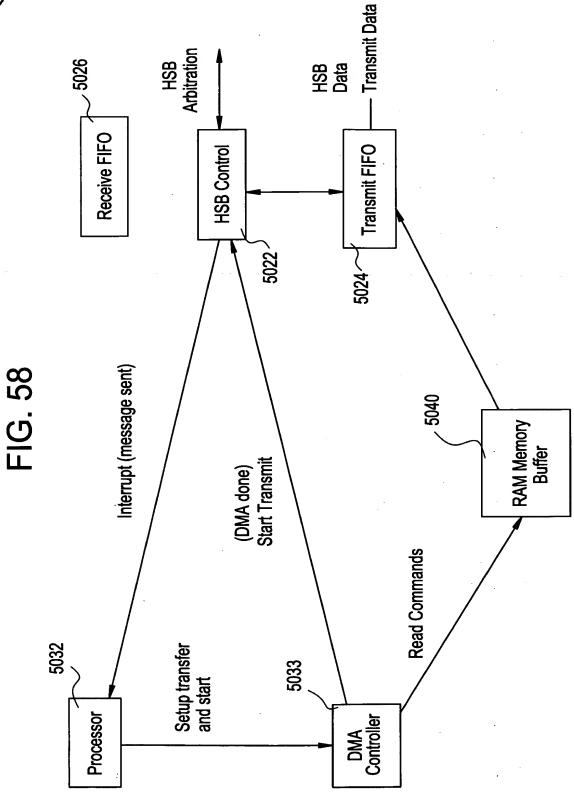


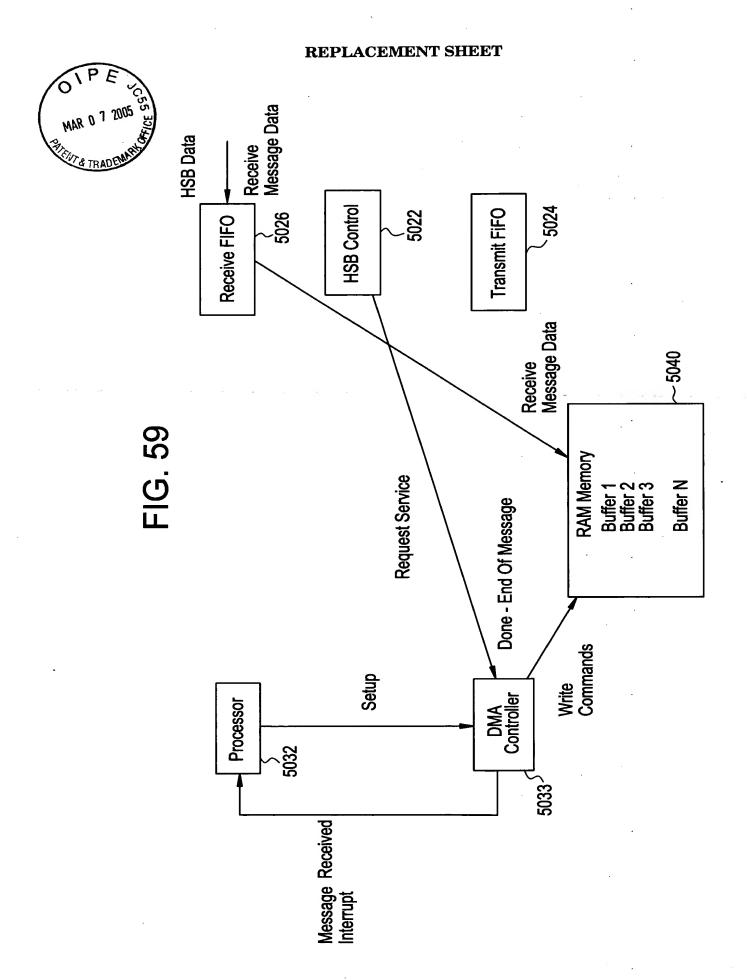
FIG. 57C



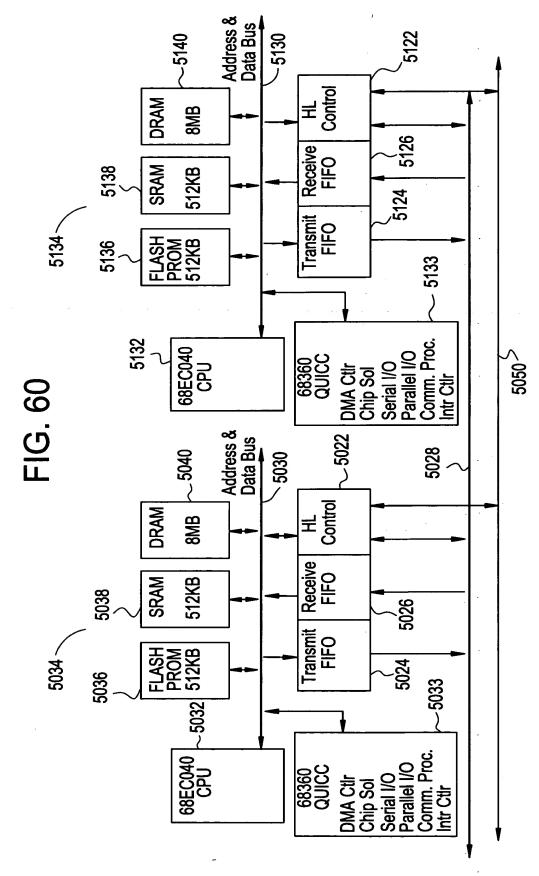












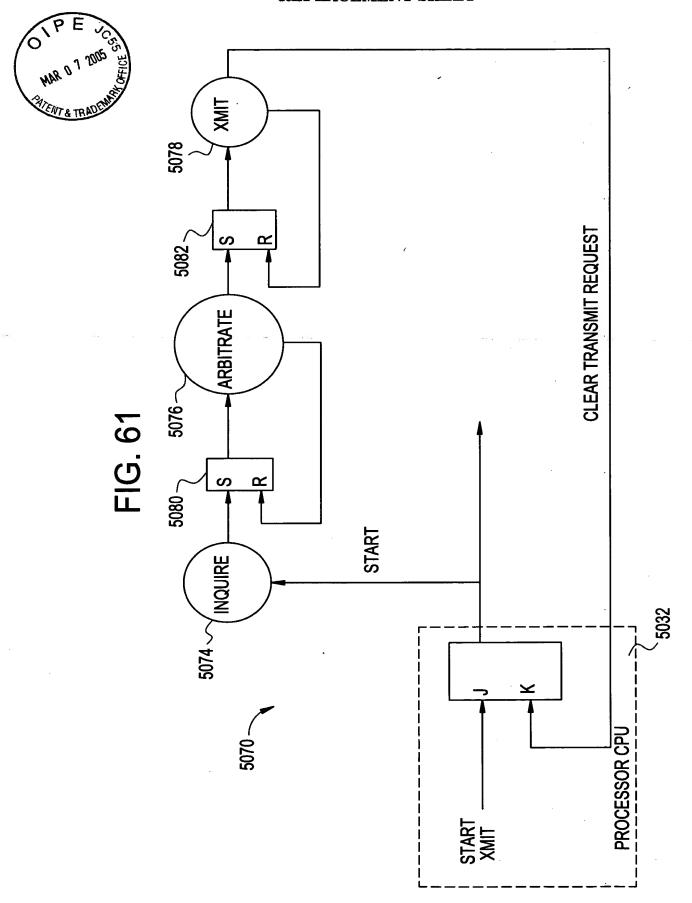




FIG. 62

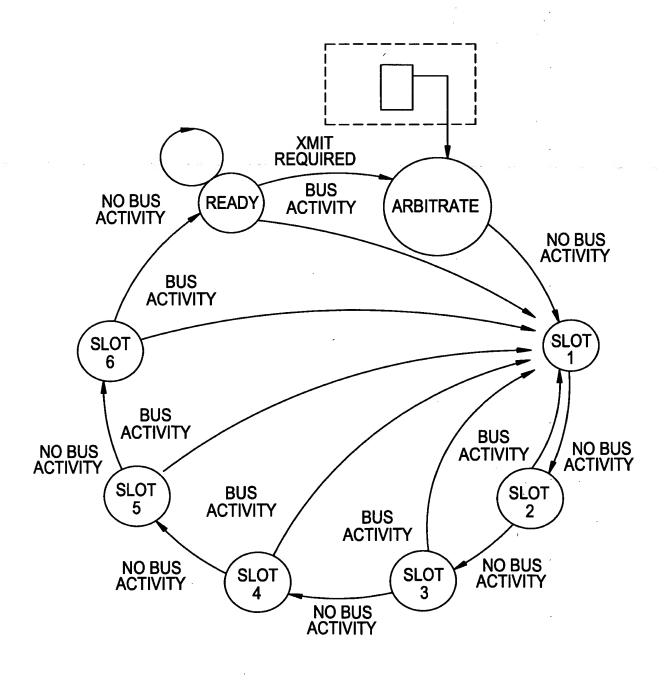




FIG. 63

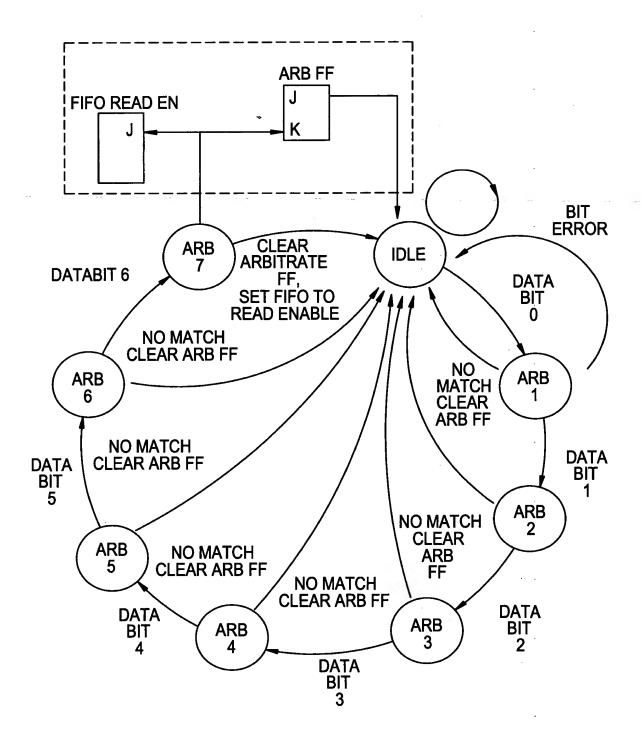




FIG. 64

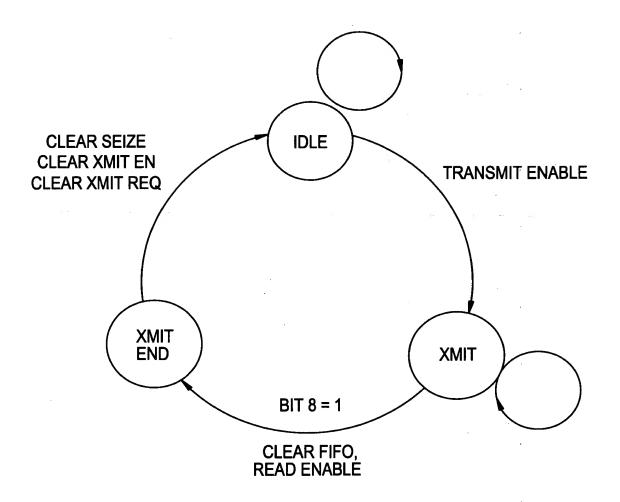


FIG. 65

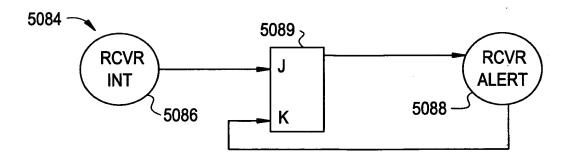




FIG. 66

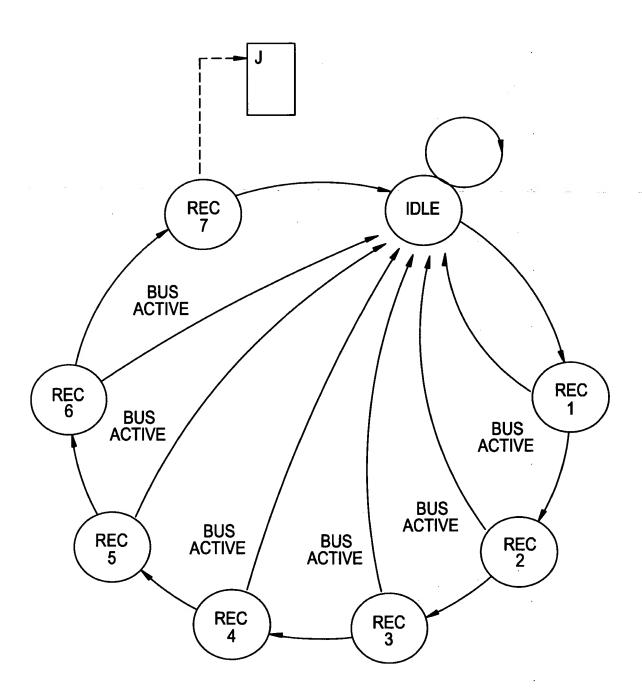
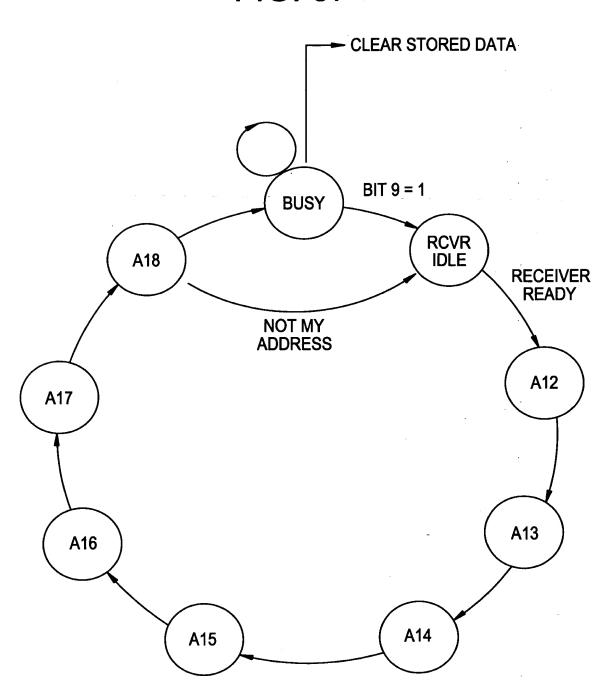




FIG. 67





## REPLACEMENT SHEET

6044

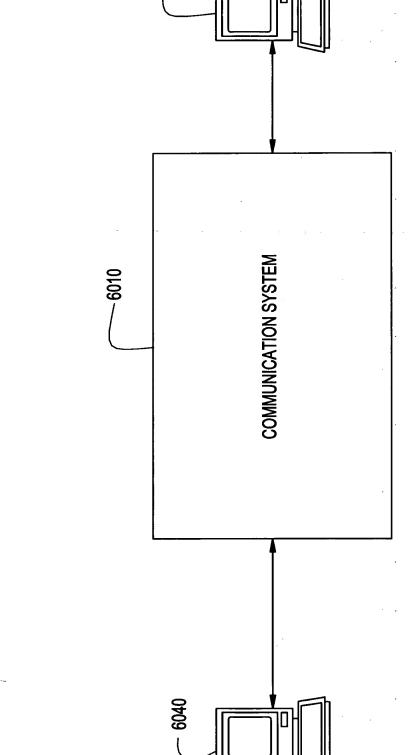
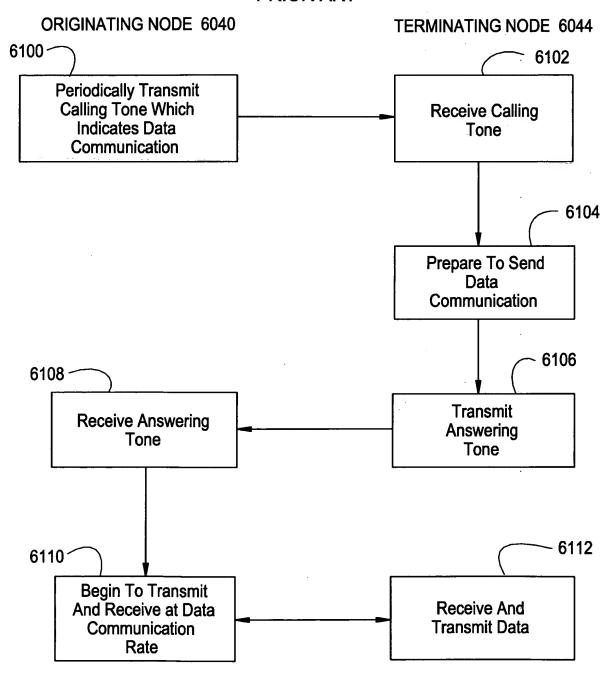


FIG. 68

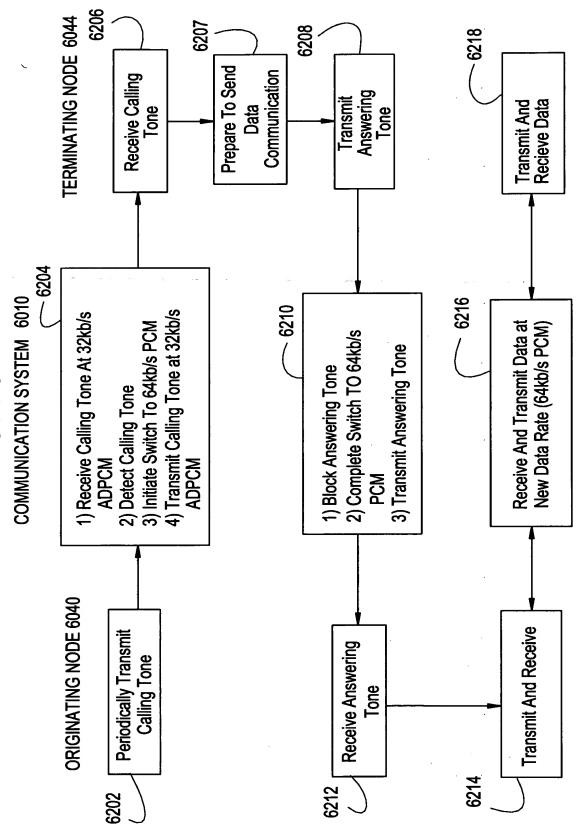


FIG. 69 PRIOR ART



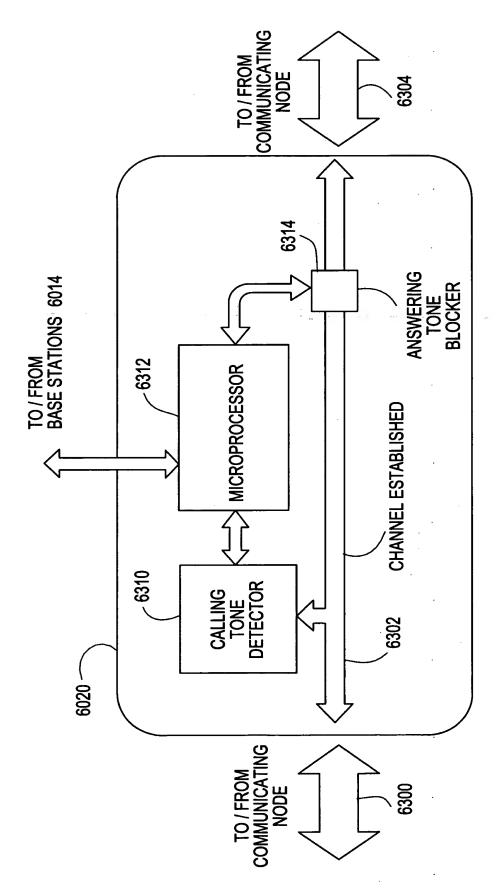




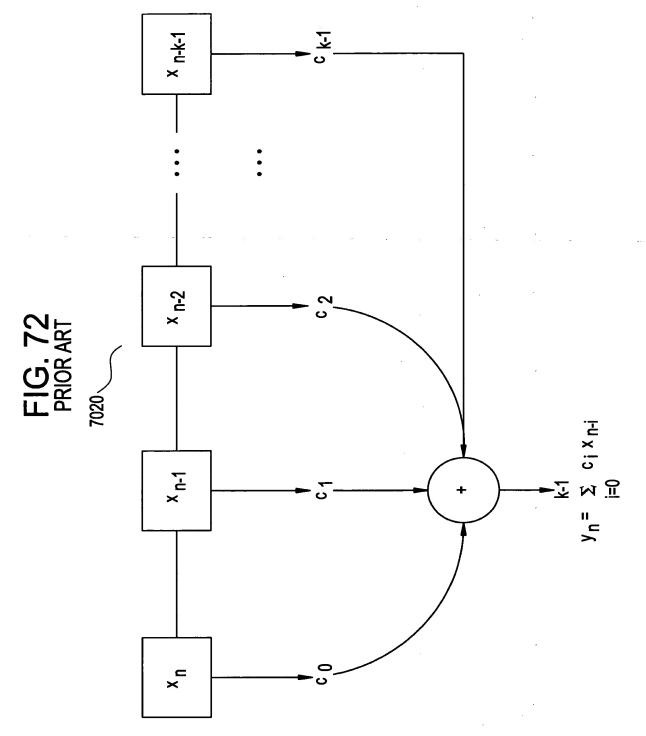


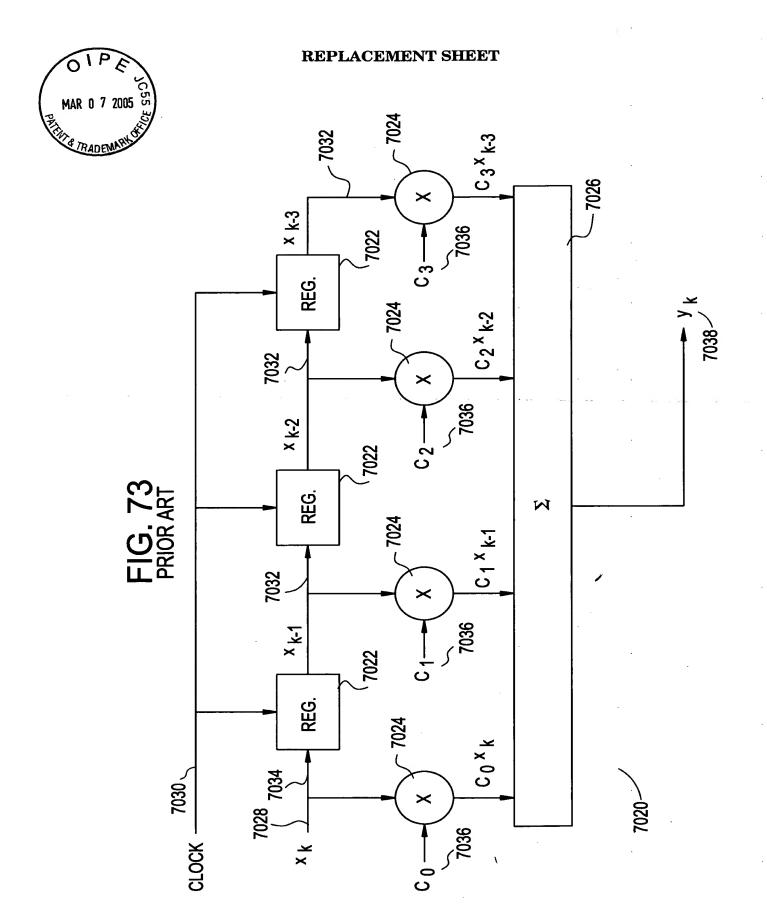














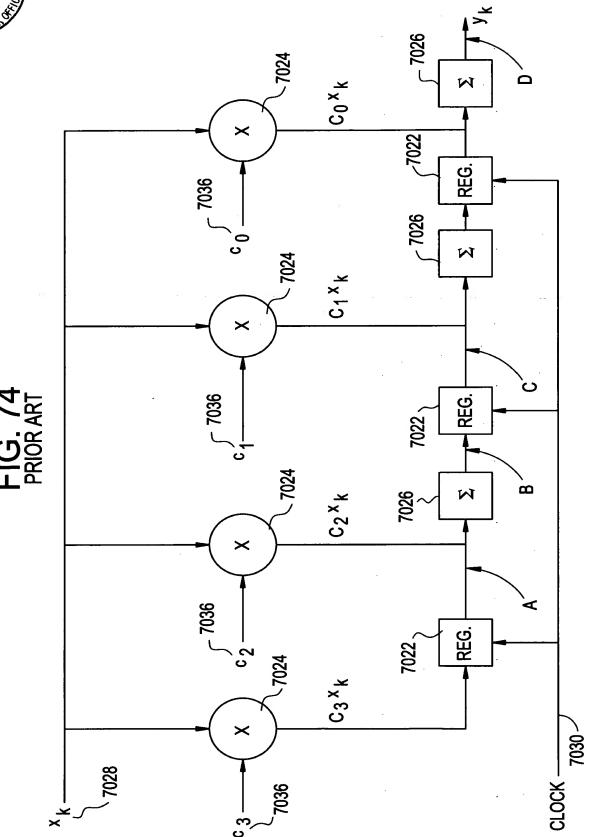
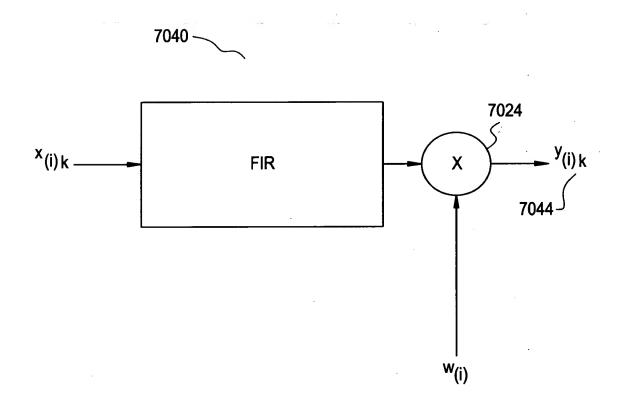
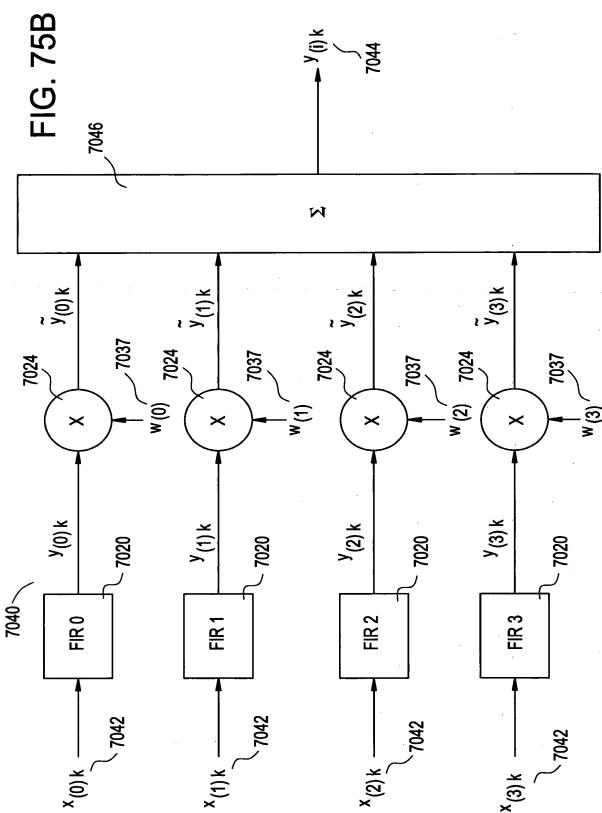




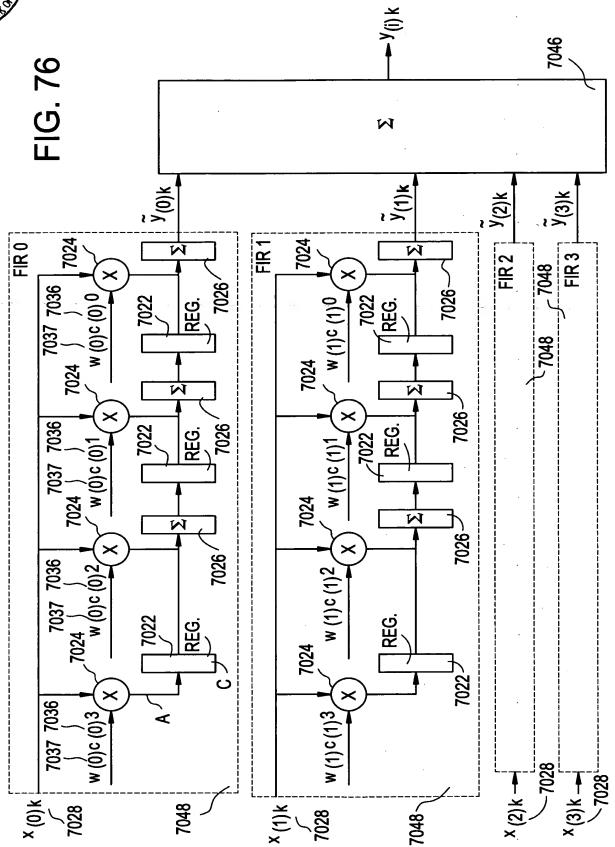
FIG. 75A







## REPLACEMENT SHEET



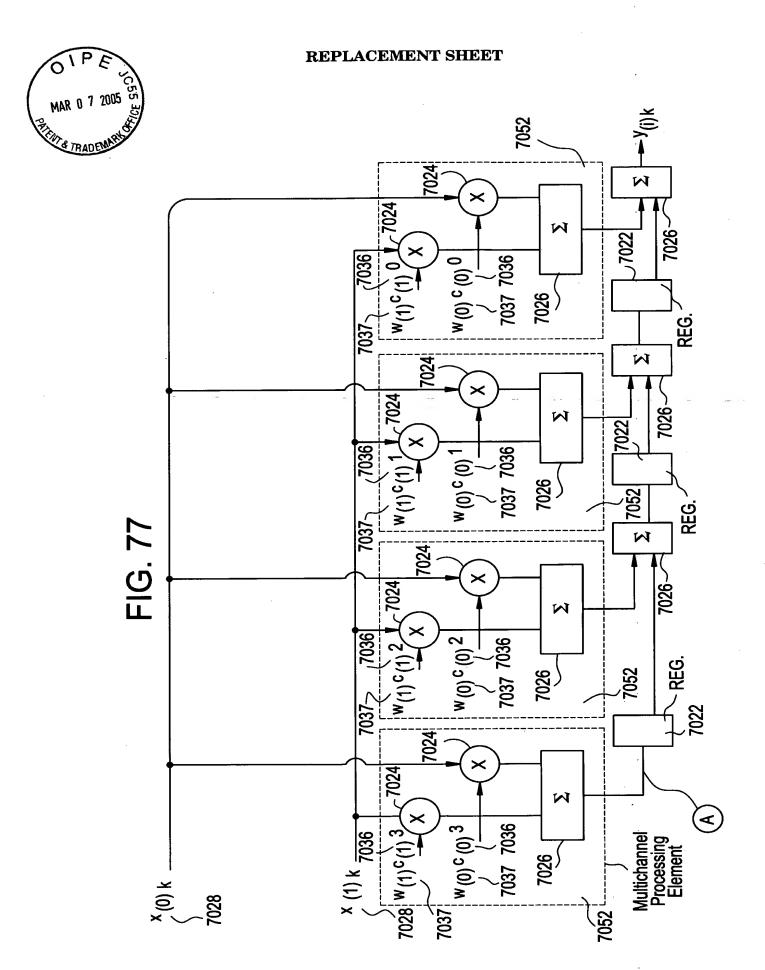




FIG. 78

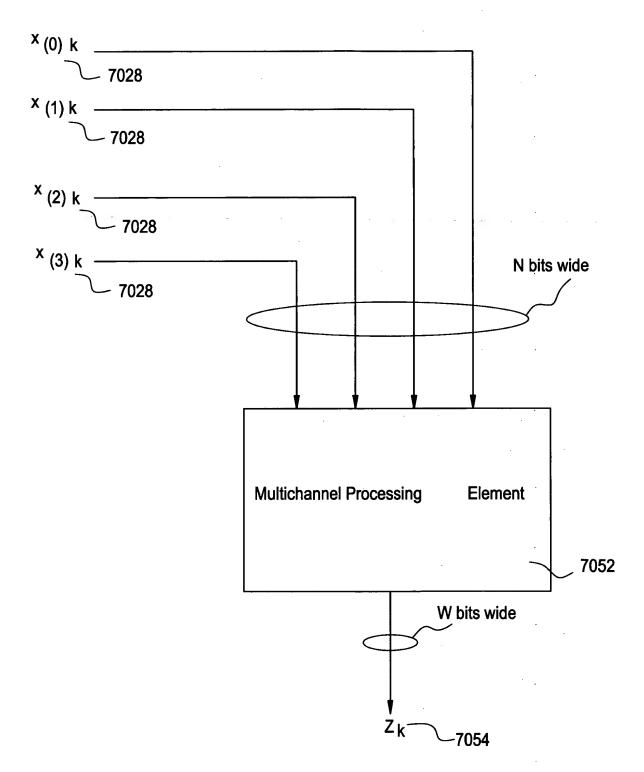
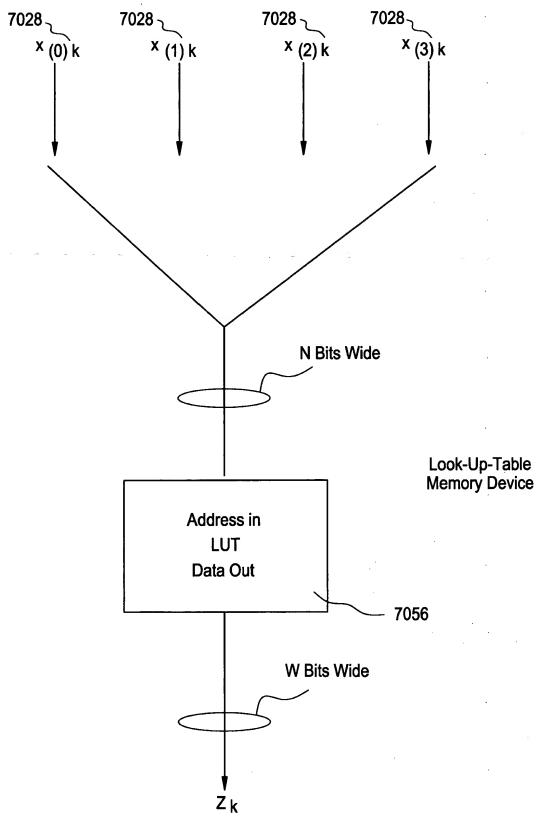
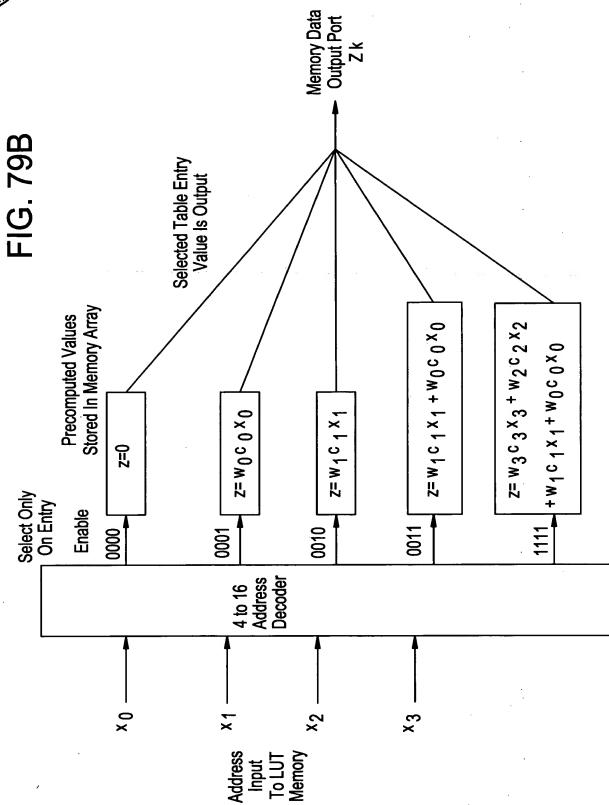


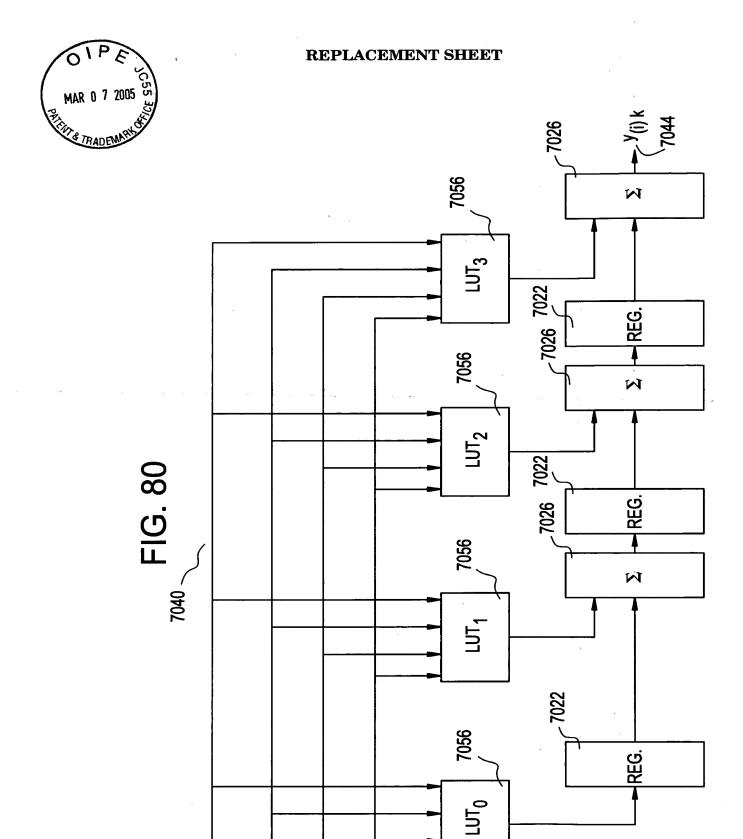


FIG. 79A









x (2) k x (3) k 7028

x (0) k — 7028